

Compal Confidential

HLXB5 MB Schematic Document

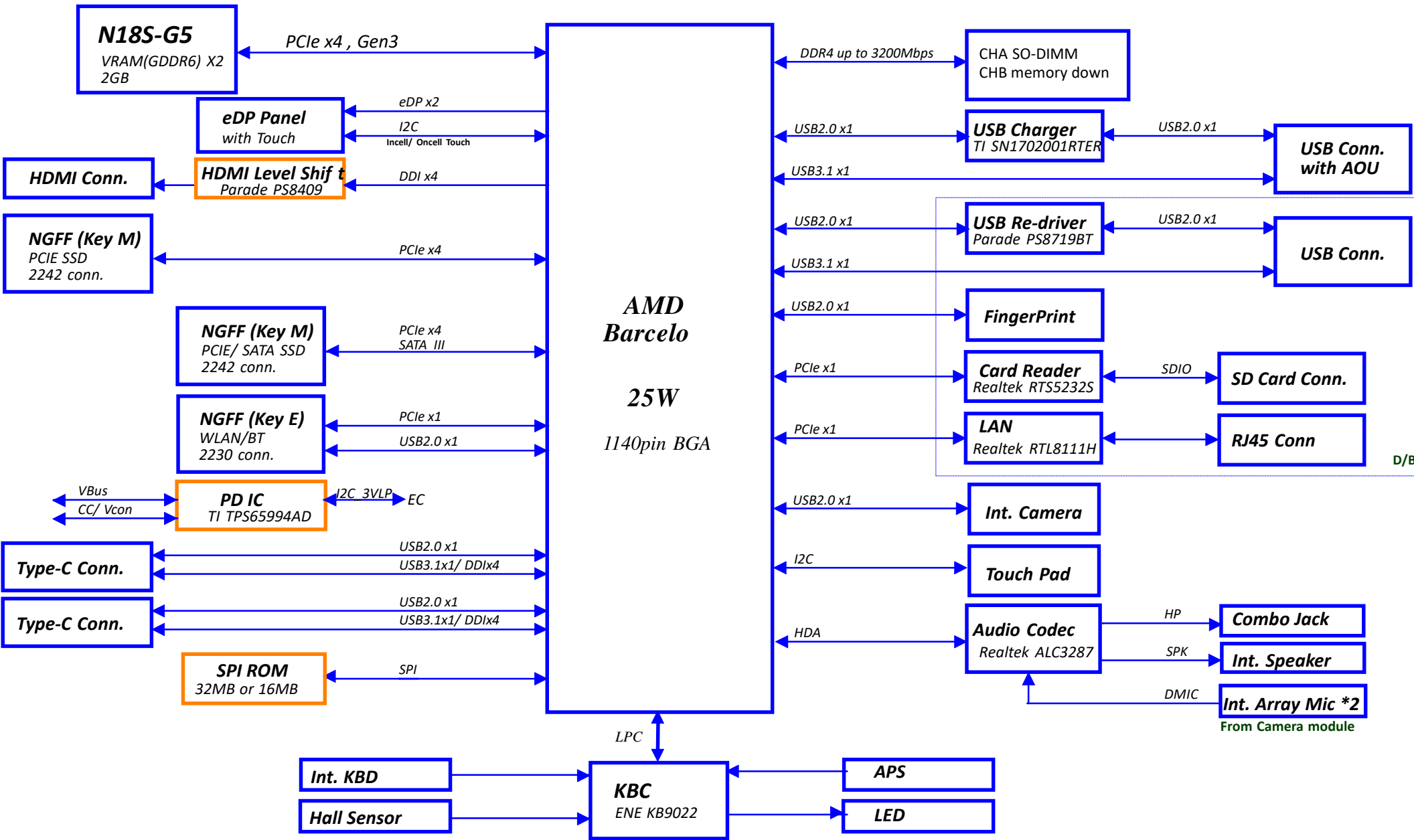
AMD Barcelo Processor with MX450

LA-M062P

Rev: 1A

2021.12.24

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Voltage Rails

power plane	+12.6VB	+5VALW +3VALW +1.8VALW +0.75VALW	+1.2V +2.5V	+5VS +3VS +1.8VS +0.75VS +0.6VS +APU_CORE +APU_CORE_SOC
State				
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EC SM Bus1 address      EC SM Bus2 address      EC SM Bus3 address

Device	Address	Device	Address	Device	Address
PD 65994AD	port A:0x20, port B:0x24	Thermal Sensor (F75305M)	1001_101xb 9Ah	Thermal Sensor (F75397M)	1001_100xb 98h
Charger (BQ25710)	0001 001x 12h	G-sensor(BMA253)	0x19	Thermal Sensor (G753T11U)	1001_000xb 90h
		GPU	0x9E		
		APU	0x98		

PCH I2C/SM Bus address

Device	Address	Device	Address
JDIMM1	0xA0	Touch pad(Synaptics)	0x2C
Touch Screen(AUO) 14"	0x39	Touch pad(ELAN)	0x15
Touch Screen(INX) 14"	0x10	Touch pad(Cirque)	0x2C
Touch Screen(BOE) 15"	0x20		
Touch Screen(IVO) 15"	0x10		

SMBUS Control Table

SOURCE	KB9022	APU	BATT	CHARGER	KB9022	PD IC	Thermal Sensor	GPU
EC_SMB_CK1	KB9022	✗	✓	✓	✓	✓	✗	✗
EC_SMB_DA1	+3VL	✓	+3VL	+3VL	+3VL	+3VL		
EC_SMB_CK2		✓	✗	✗	✓	✗	✓	✓
EC_SMB_DA2	+3VS	+3VS			+3VS		+3VS	+1.8VGS AON

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Table

Item	BOM Structure
Memory Down - SDP Package	SDP@
Memory Down - DDP Package	DDP@
Keyboard BackLight	KBL@
Finger Print	FP@
Non Finger Print SKU	NONFP@
Touch Screen	TOUCH@
SSD2 SKU	SSD2@
UMA SKU	UMA@
GPU SKU	DIS@
GC6 SKU	GC6@
TPM SKU	TPM@
NON TPM SKU	NONTPM@
Nuvton TPM	Nuvton@
ST TPM	ST@
Nations TCM	Nations@
APS SKU	APS@
NONAPS SKU	NONAPS@
AOU SKU	AOU@
NONAOU SKU	NONAOU@
EMI pop	EMI@
EMI un-pop	@EMI@
ESD pop	ESD@
ESD un-pop	@ESD@
RF pop	RF@
RF un-pop	@RF@
Debug	HDT@
memory down relative parts	X76@
EMI ESD parts for 14	X4E_14@
EMI ESD parts for 15	X4E_15@
PCB 14 DA P/N	14@
PCB 15 DA P/N	15@

USB 2.0 Port Table

Port	External USB Port
0	USB2/3 Port (Type-C1)
1	USB2/3 Port (IO - 1)
2	Camera
3	
4	USB2/3 Port (Type-C2)
5	USB2/3 Port (IO - 2)
6	Fingrt Print
7	NGFF BT

USB 3.0 Port Table

Port	External USB Port
0	USB2/3 Port (Type-C1)
1	USB2/3 Port (IO - 1)
4	USB2/3 Port (Type-C2)
5	USB2/3 Port (IO - 2)

DDI Port Table

Port	Lane
0	eDP
1	HDMI
2	TYPE C1 (PD + CC)
3	TYPE C2 (PD + CC)

GPP Port Table

Port	Lane	
0	0	
1	1	
2	2	
3	3	
4	4	CardReader
5	5	LAN
6	6	NGFF WLAN
7	7	
8	8	
9	9	
10	10	
11	11	

XTAL RAM X76

X76 X76_3215@  X76 CRYSTAL_3215 X7695138059	X76 X76_2012@  X76 CRYSTAL_2012 X7695138060
--	--

APU P/N

UC1 C3@  R/ZEN3 100-000000586 2.7G SA0001EX709	UC1 C5@  RYZEN5 100-000000583 2.3G SA0001EX709	UC1 C7@  R/ZYEN7 100-000000580 2G SA0001EX721
---	---	--

GPU P/N

UV1  SA0000DGW50 SIC N18S-G5-A1 BGA 603P MP C38 I D6@
--

ON BOARD RAM X76

X76 X76_S4G@  X76 SAMSUNG 4GB SINGEL X7695138051	X76 X76_H4G@  X76 HYNIX 4GB SINGEL X7695138052	X76 X76_M4G@  X76 MICRON 4GB SINGEL X7695138053
X76 X76_S8G@  X76 SAMSUNG 8GB DUAL X7695138054	X76 X76_H8G@  X76 HYNIX 8GB DUAL X7695138055	X76 X76_M8G@  X76 MICRON 8GB DUAL X7695138056

DAZ PN

ZZZ 14@  PCB HLXB4 LA-M062P LS-K051P/K053P 10 DAZ35000500 ZZZ 15@  PCB HLXB5 LA-M062P LS-K056P/K057P 102 DAZ35000101
---

X4E

X4E X4E_14@  SMT EMC FOR EE M/B 14" LAM061 HLXB4 X4EAV038U1	X4E X4E_15@  SMT EMC FOR EE M/B 15 LAM062 HLXB5 X4EAV038U1
--	---



Power Sequence

Boot

Shut  
Down

EC Pin 110 Input

EC Pin 112 Output

AC Plug

EC Pin 114 Input

EC Pin 100 Output

EC Pin 122 Output

EC Pin 123 Input

EC Pin 6 Input

EC Pin 95 Output

EC Pin 116 Input

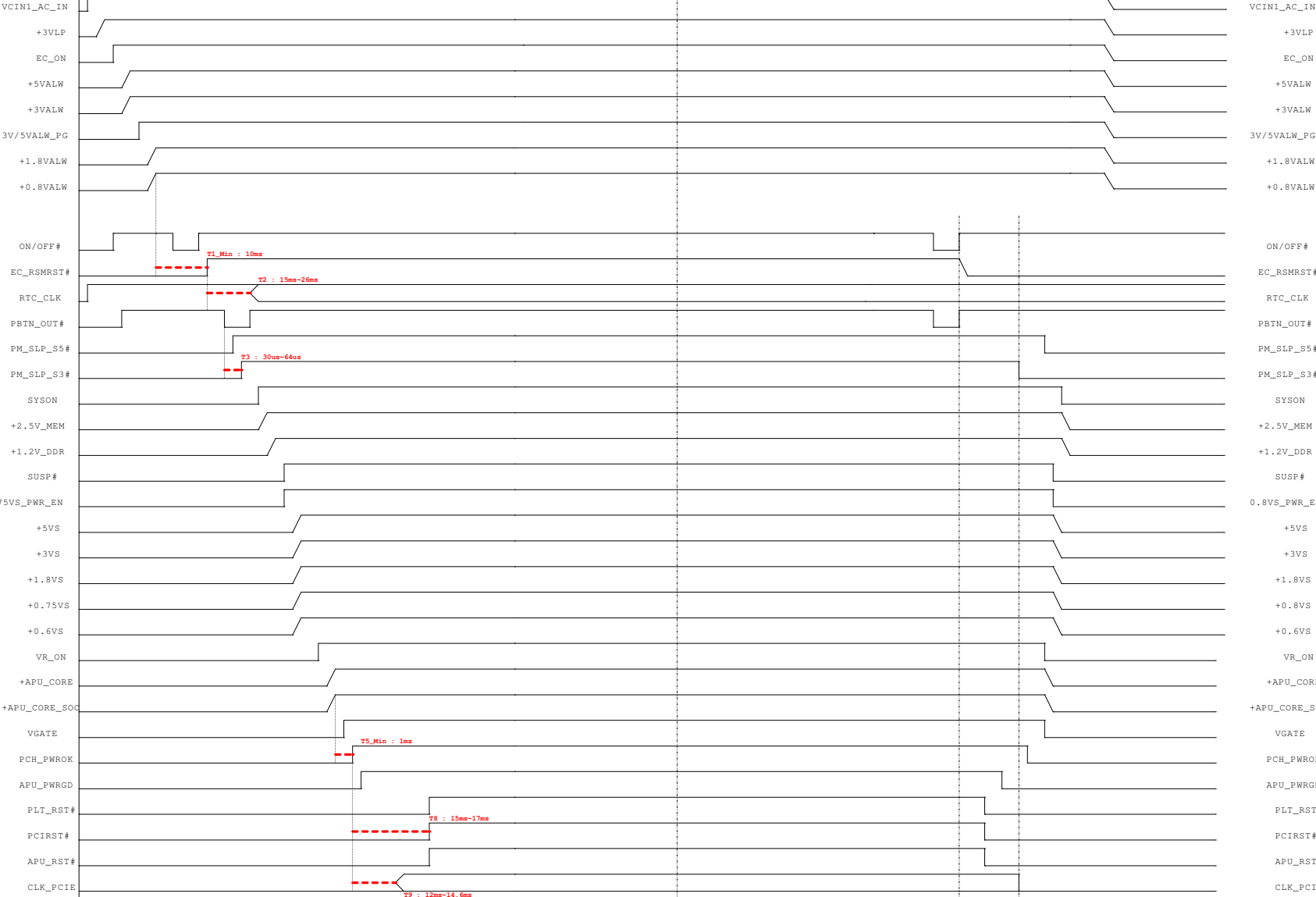
EC Pin 99 Output

EC Pin 121 Output

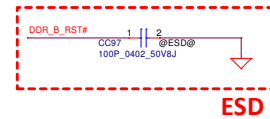
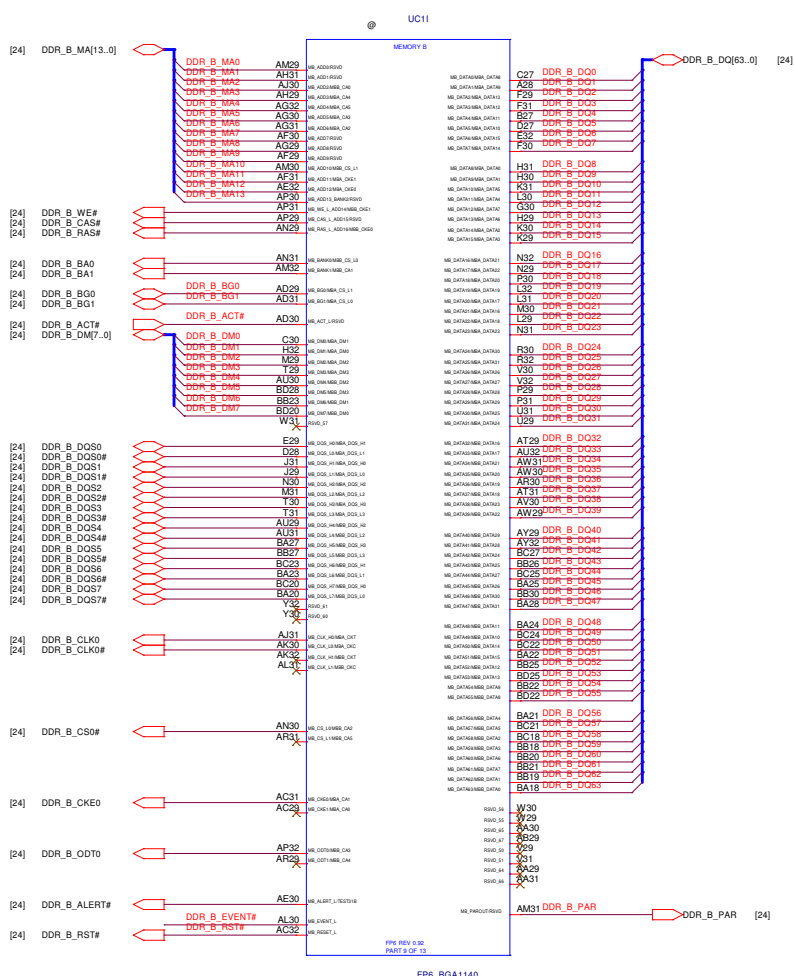
EC Pin 36 Input

EC Pin 32 Output

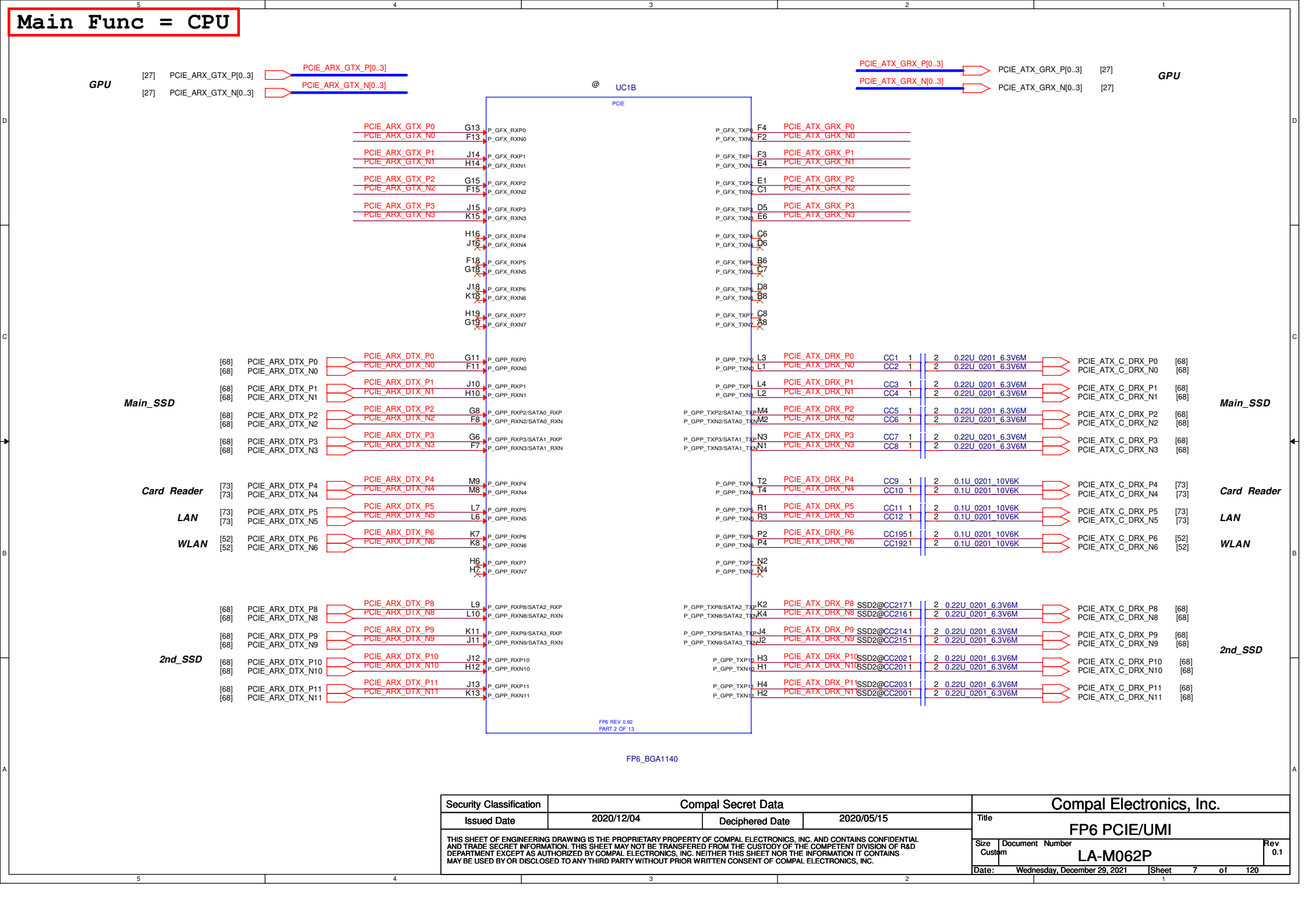
EC Pin 13 Input



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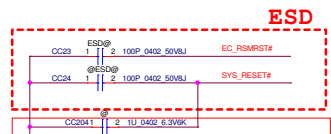
Main Func = CPU



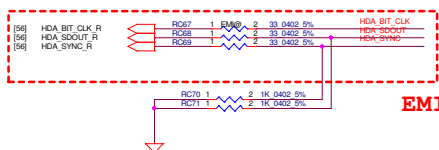
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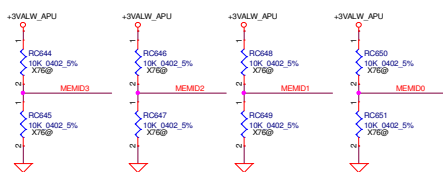


Reserver for Check list

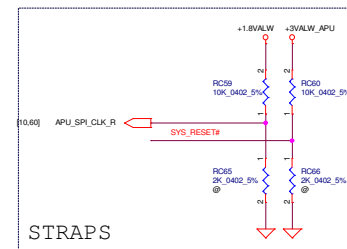
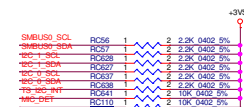
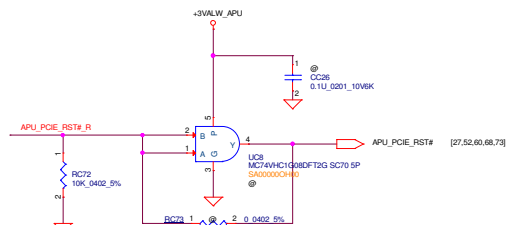
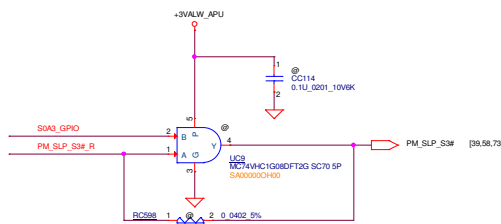
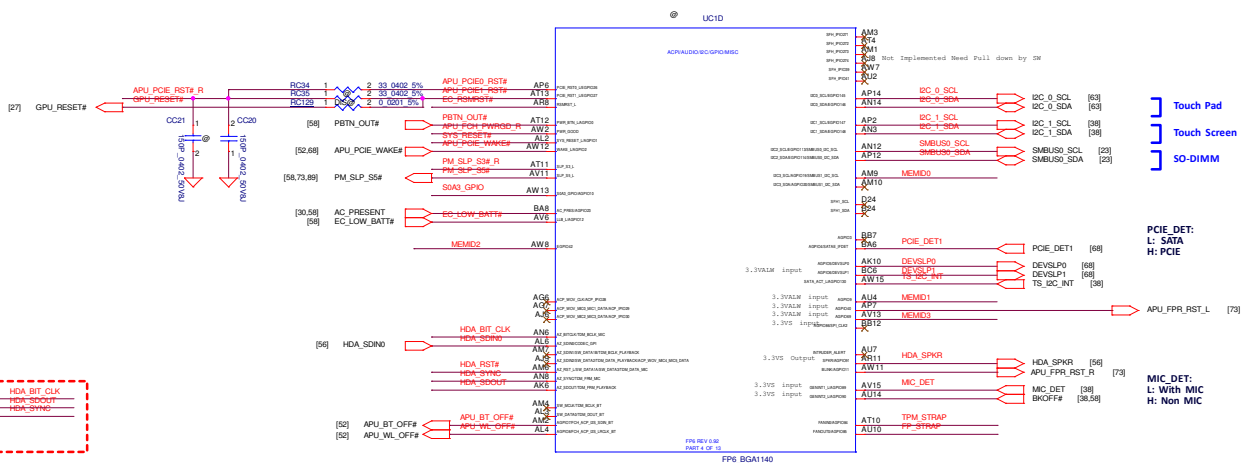


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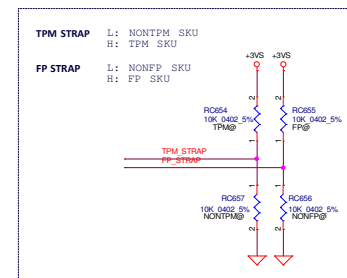
[REDACTED]		Total	Description	OBRAM_ID3	OBRAM_ID2	OBRAM_ID1	[REDACTED]_ID0	Compal P/N
8Gb-3200	4GB	Samsung K4A8G165WC-BCWCE SDP		0	0	0	0	SA0000CZ500
		Hynix H5AN8G6NDJR-XNC SDP		0	0	0	1	SA0000CZ330
		Micron MT40A512M16TB-062E-R SDP		0	0	1	0	SA0000CMS60
16Gb-3200	8GB	Samsung K4AAG165WB-BCWCE SDP		0	0	1	1	SA0000CZ250
		Hynix H5ANAG6NCJR-XNC SDP		0	1	0	0	SA0000DYB00
		Micron MT40A1G16TB-062E:F SDP		0	1	0	1	SA0000F5300



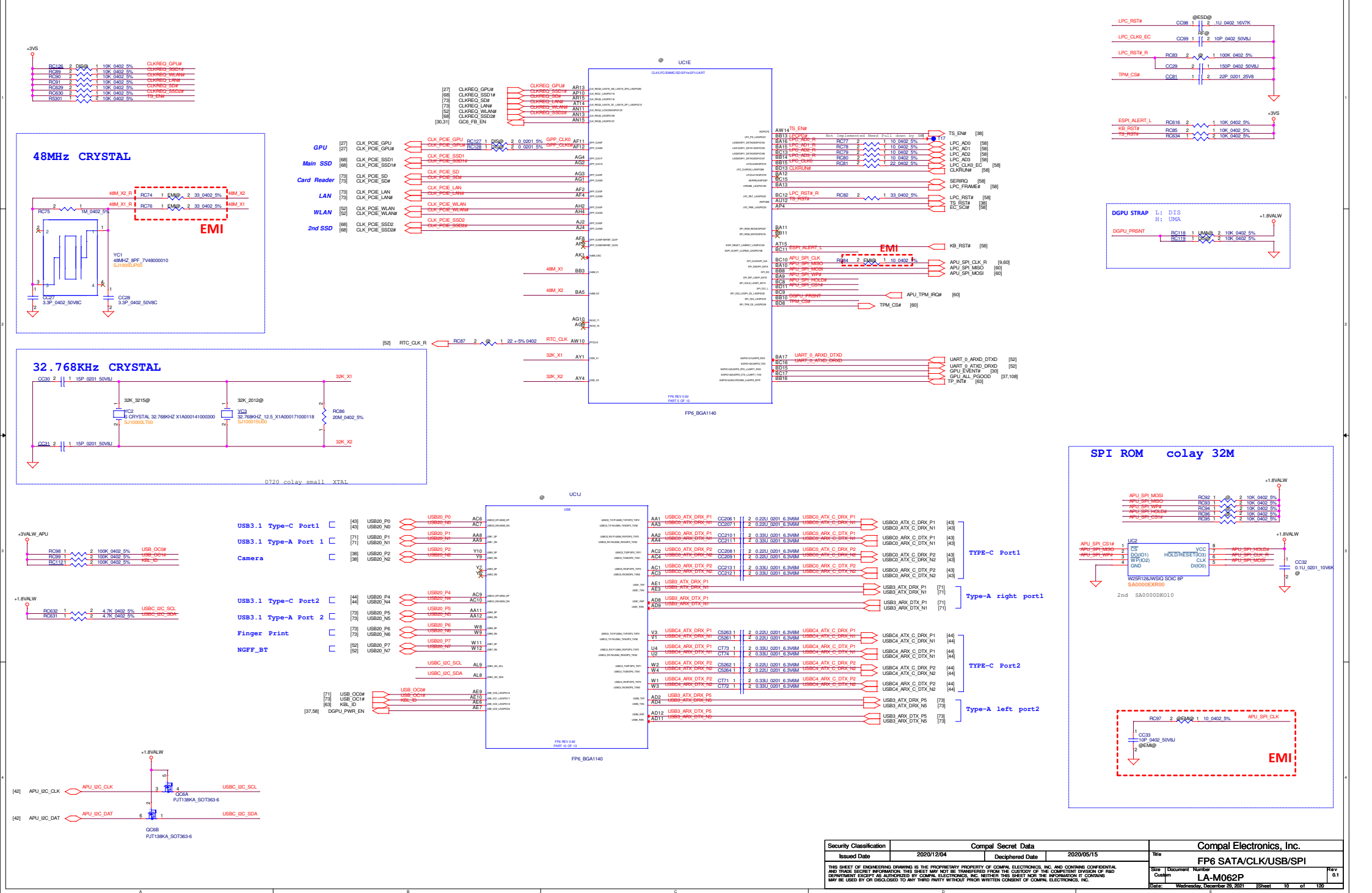
MEM ID



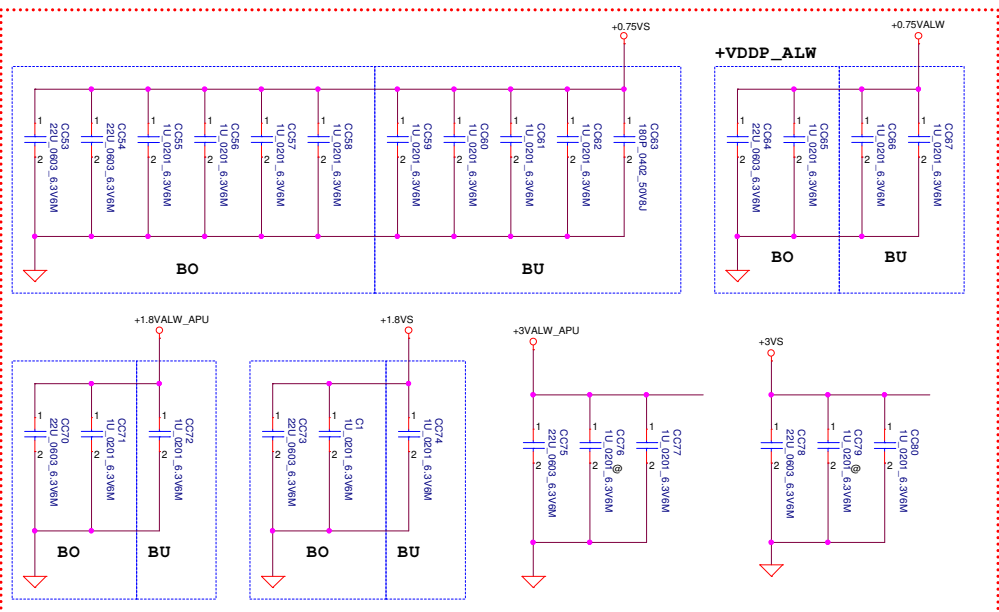
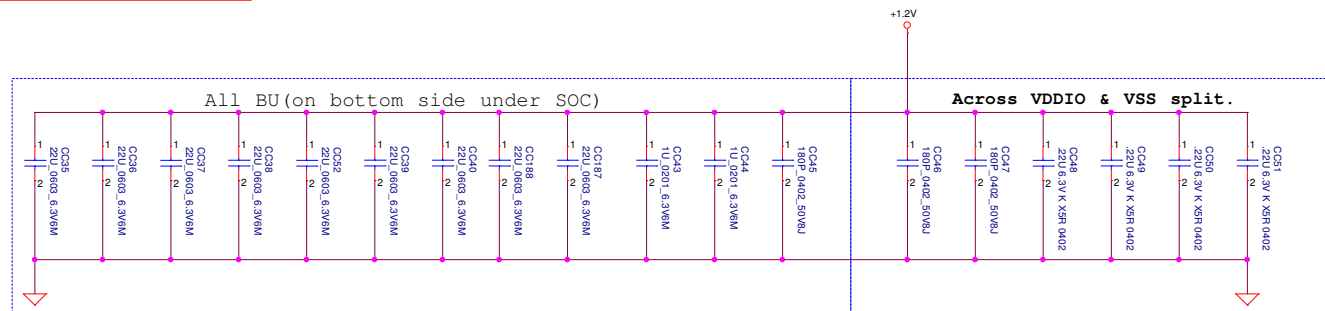
STRAPS	DEFINITION
SPI_CLK	1 : Use 48MHZ Crystal Clock and Generate both internal and external clocks (Default) 0 : Use 100MHZ PCIE clock as reference clock and generate internal clocks only
SYS_RST#	1 : Normal reset mode (Default) 0 : short reset mode



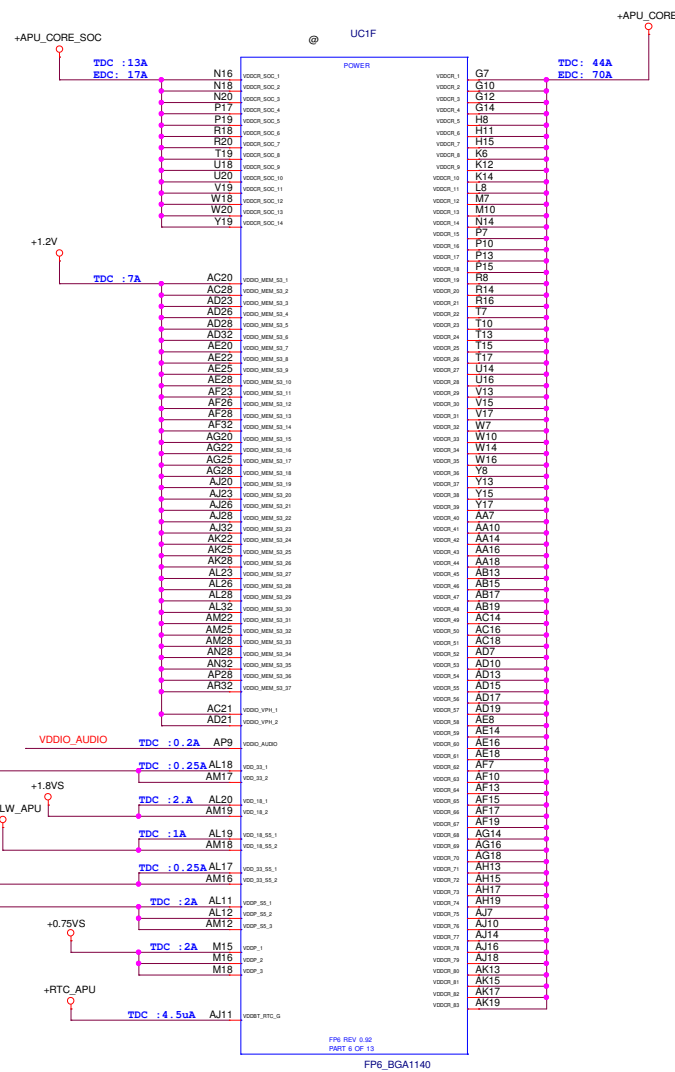
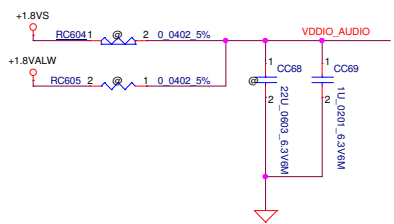
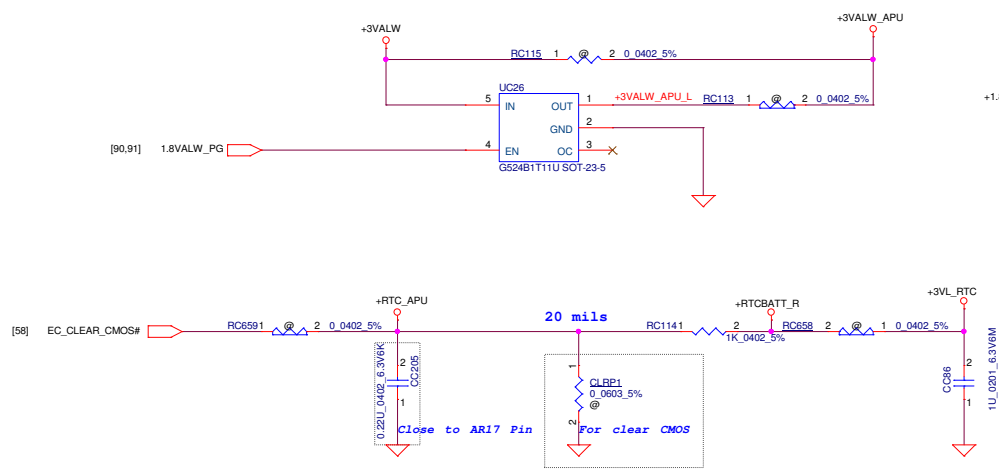
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Date	Wednesday	May 6, 2021	Issued at	150

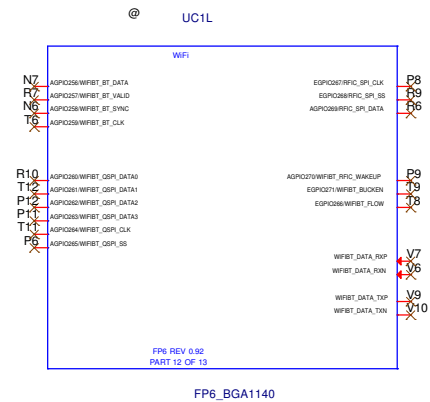
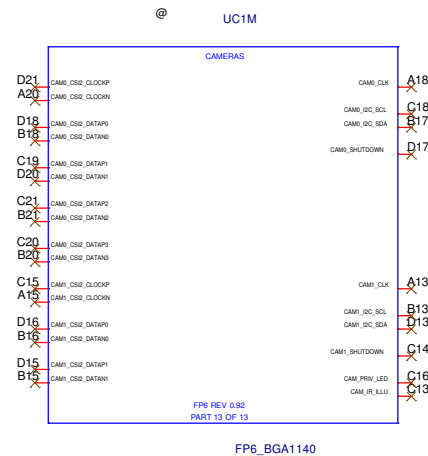


Main Func = CPU

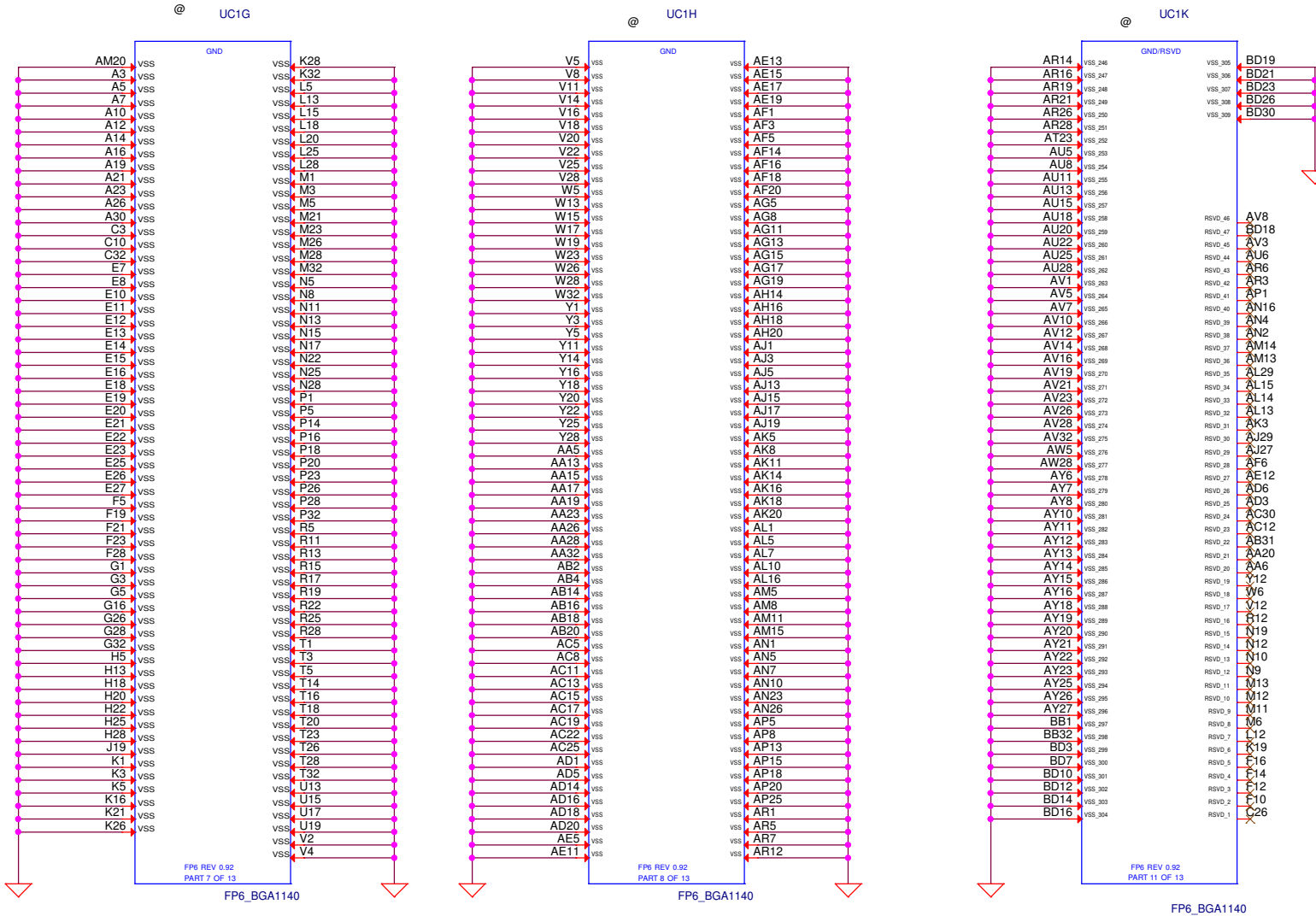


Note : Cap placemet need to close APU





Main Func = CPU



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D

D

C

C

B

B

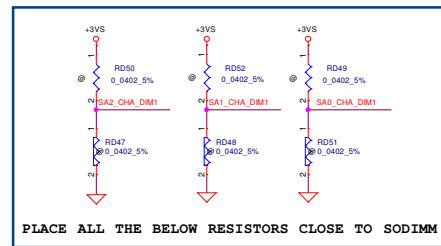
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## CHANNEL-A

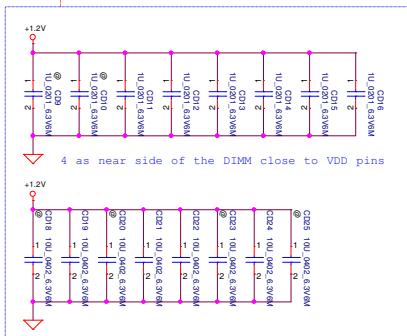
JDIMM1 ADDRESS (PLACE CLOSE TO DIMM)



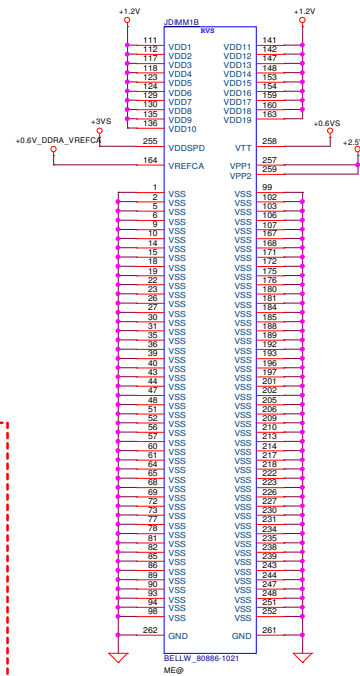
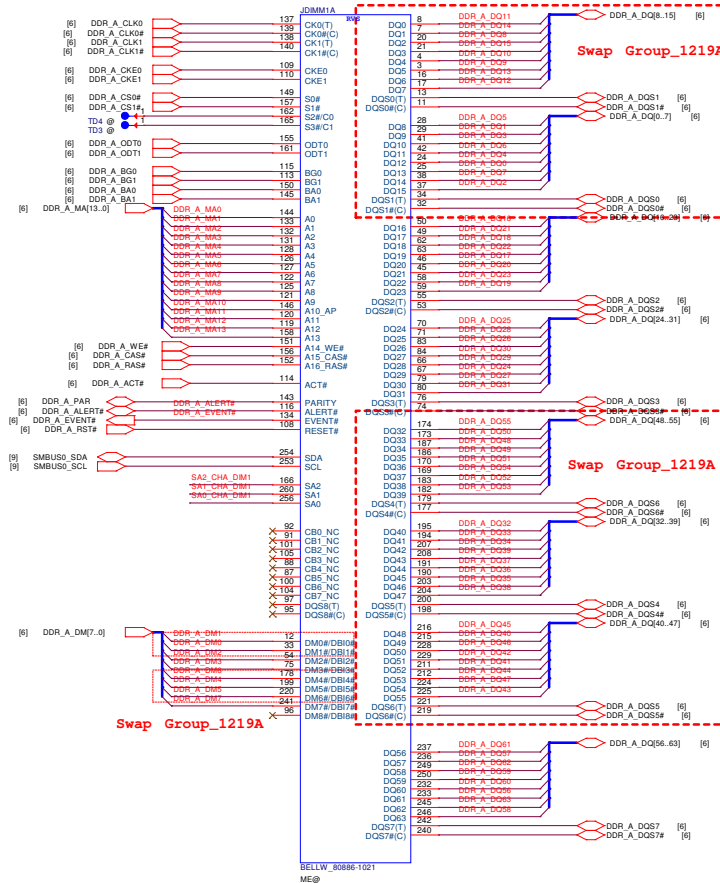
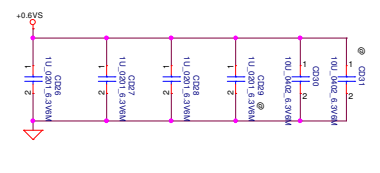
```
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS:
READ ADDRESS:
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S
```



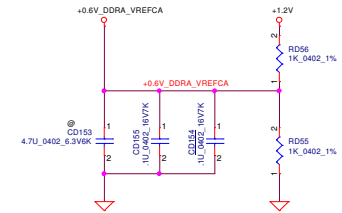
Layout Note:  
Place near JDIMM1



Place these caps on the VTT plane close to DIMM

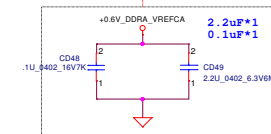


<b>Standard Type</b> 2-3A to 1 DIMMs/channel
---

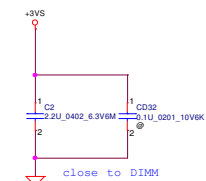
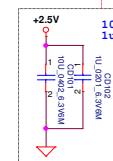


Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket

Layout Note:  
PLACE THE CAP WITHIN 200 MILS  
FROM THE JDIMM2

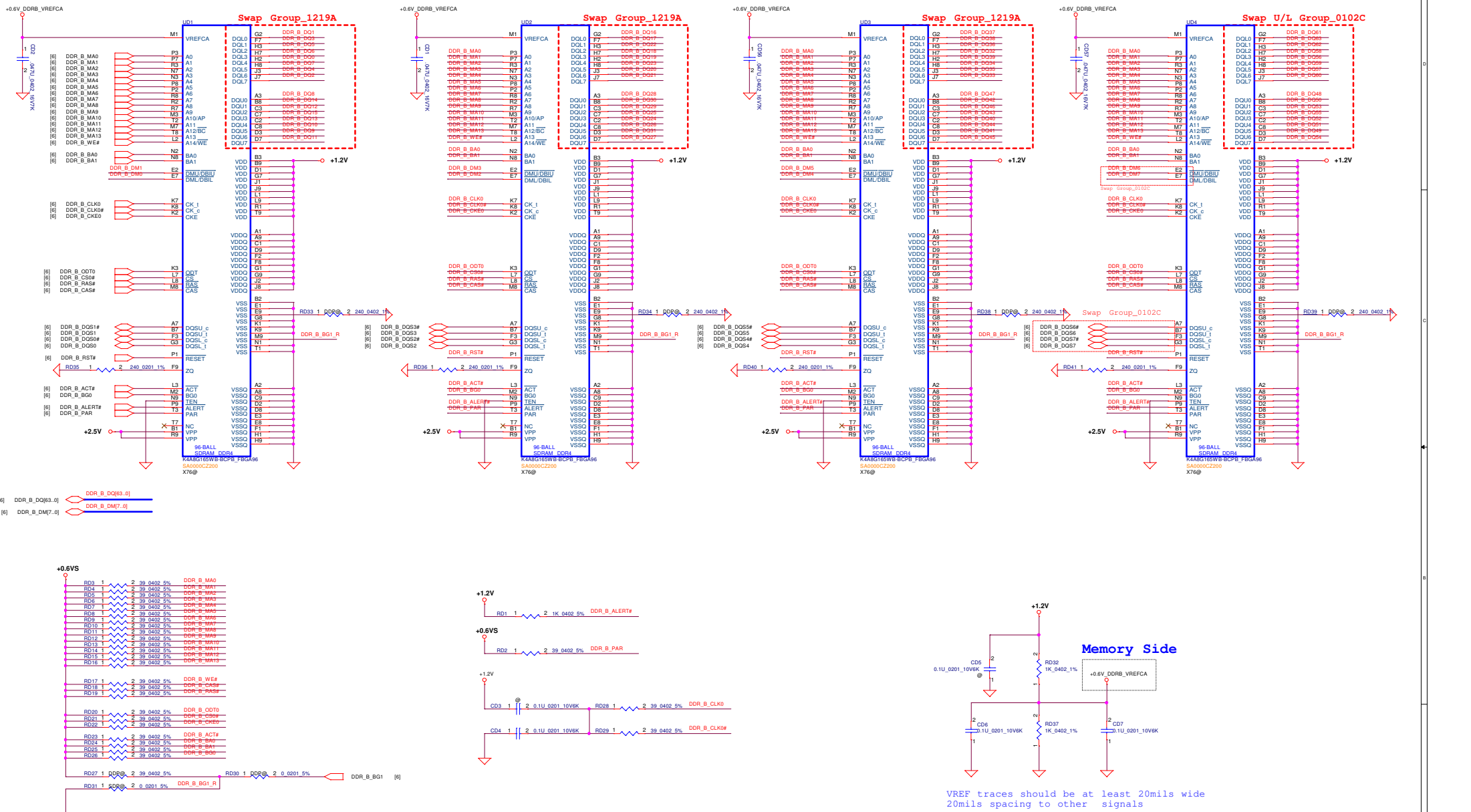


Layout Note:  
Place near JDIMM2



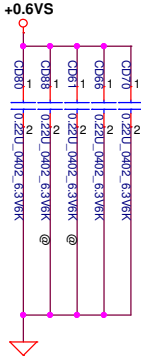
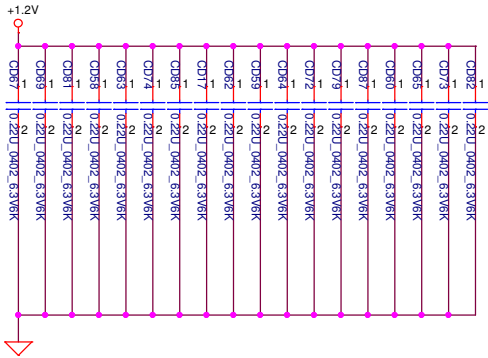
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CHANNEL-B

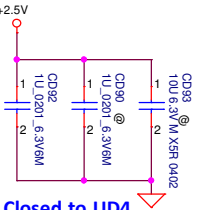
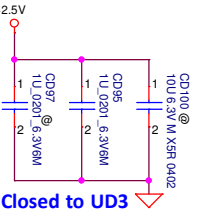
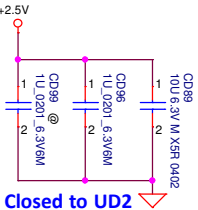
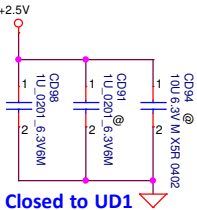
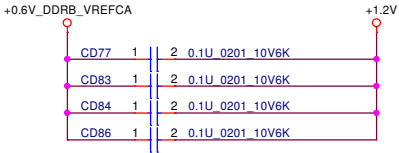
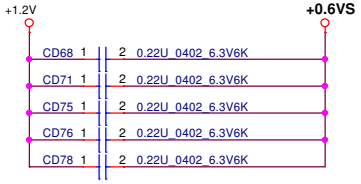
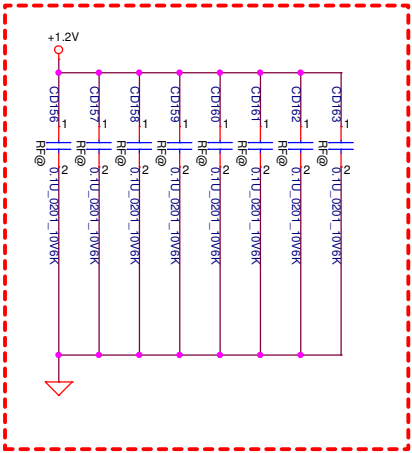




DRAM DOWN DECOUPLING



RF requirement\_0407A



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**GPU**

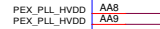
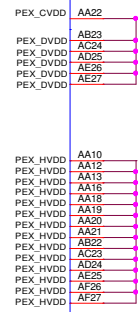
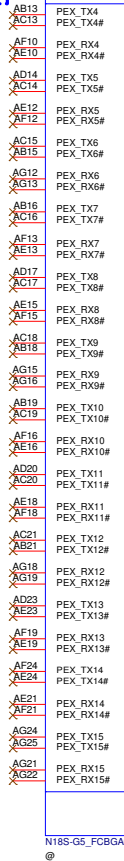
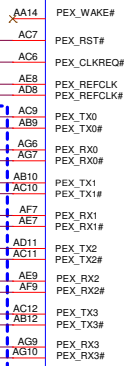
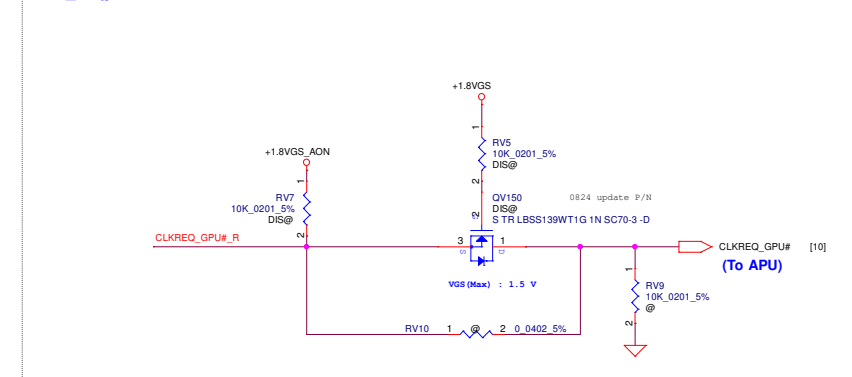
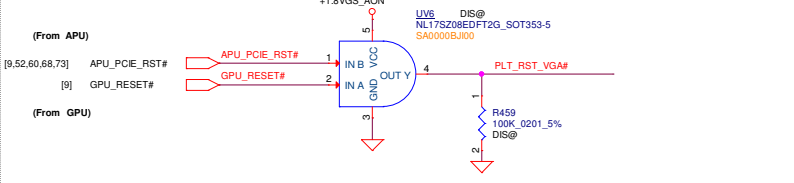
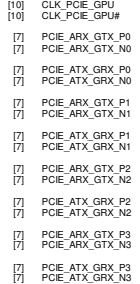
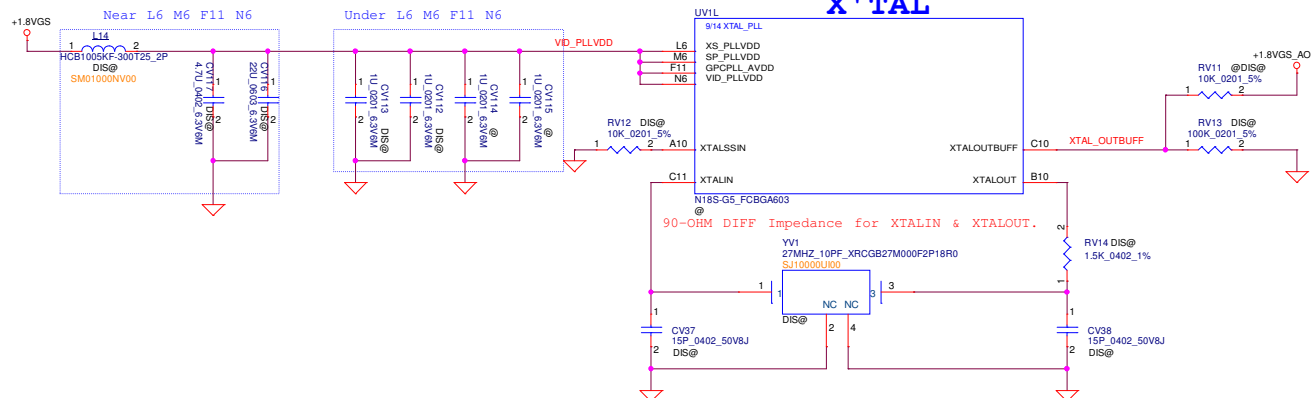
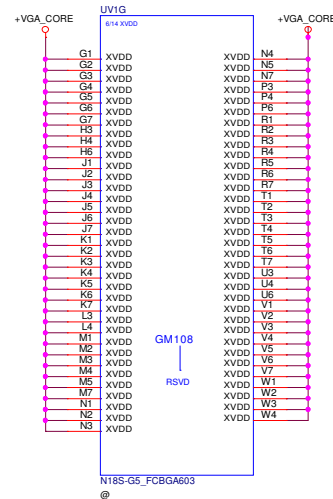
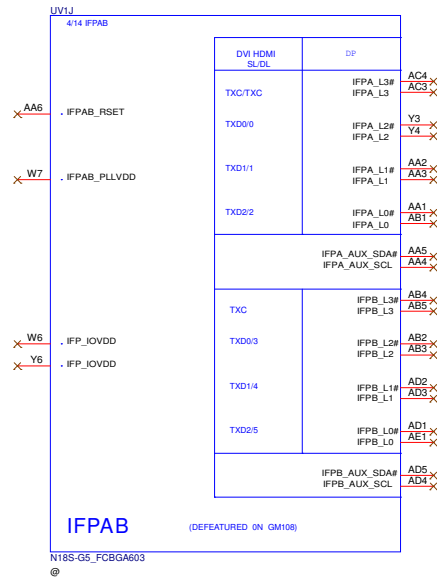
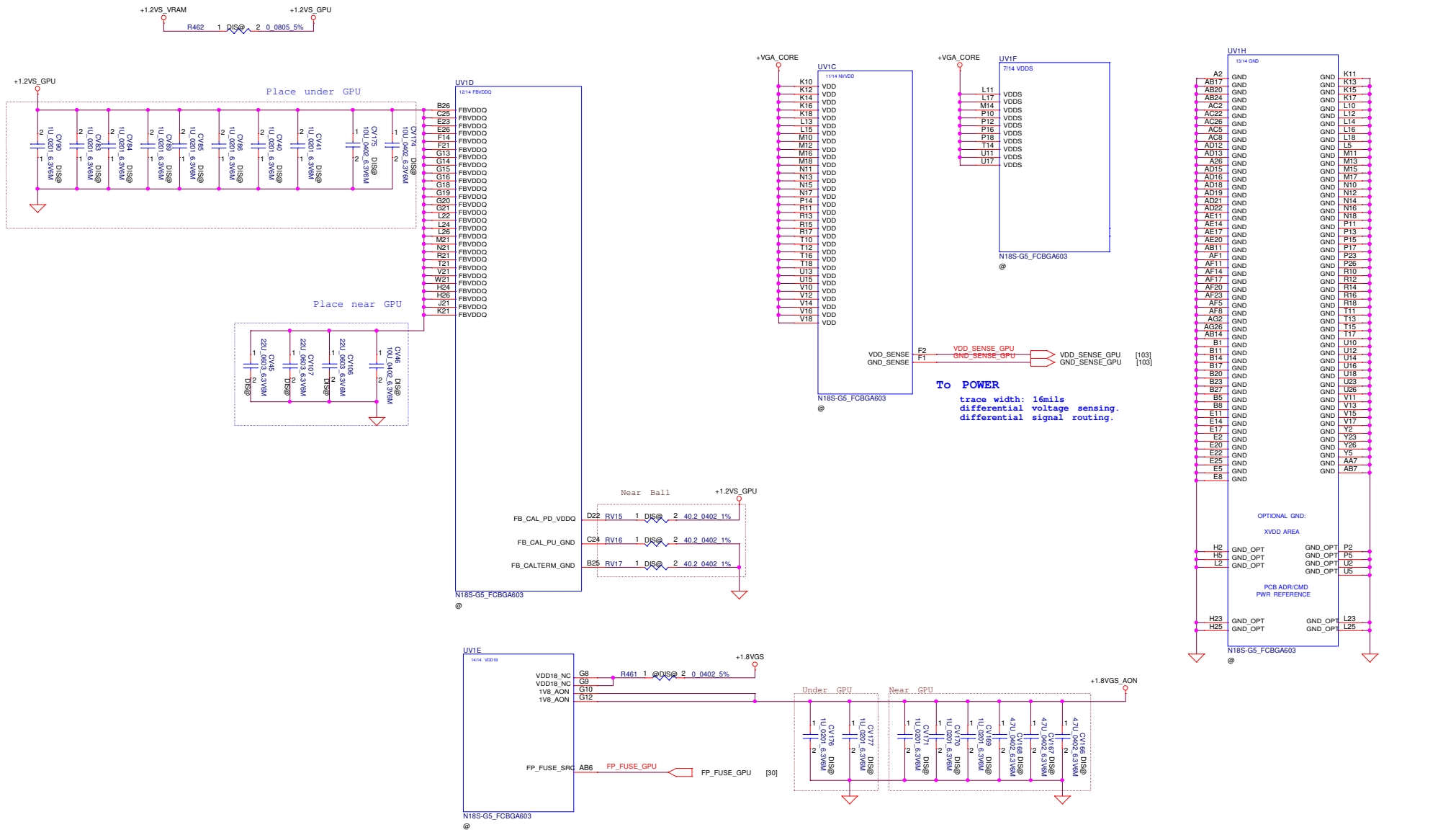


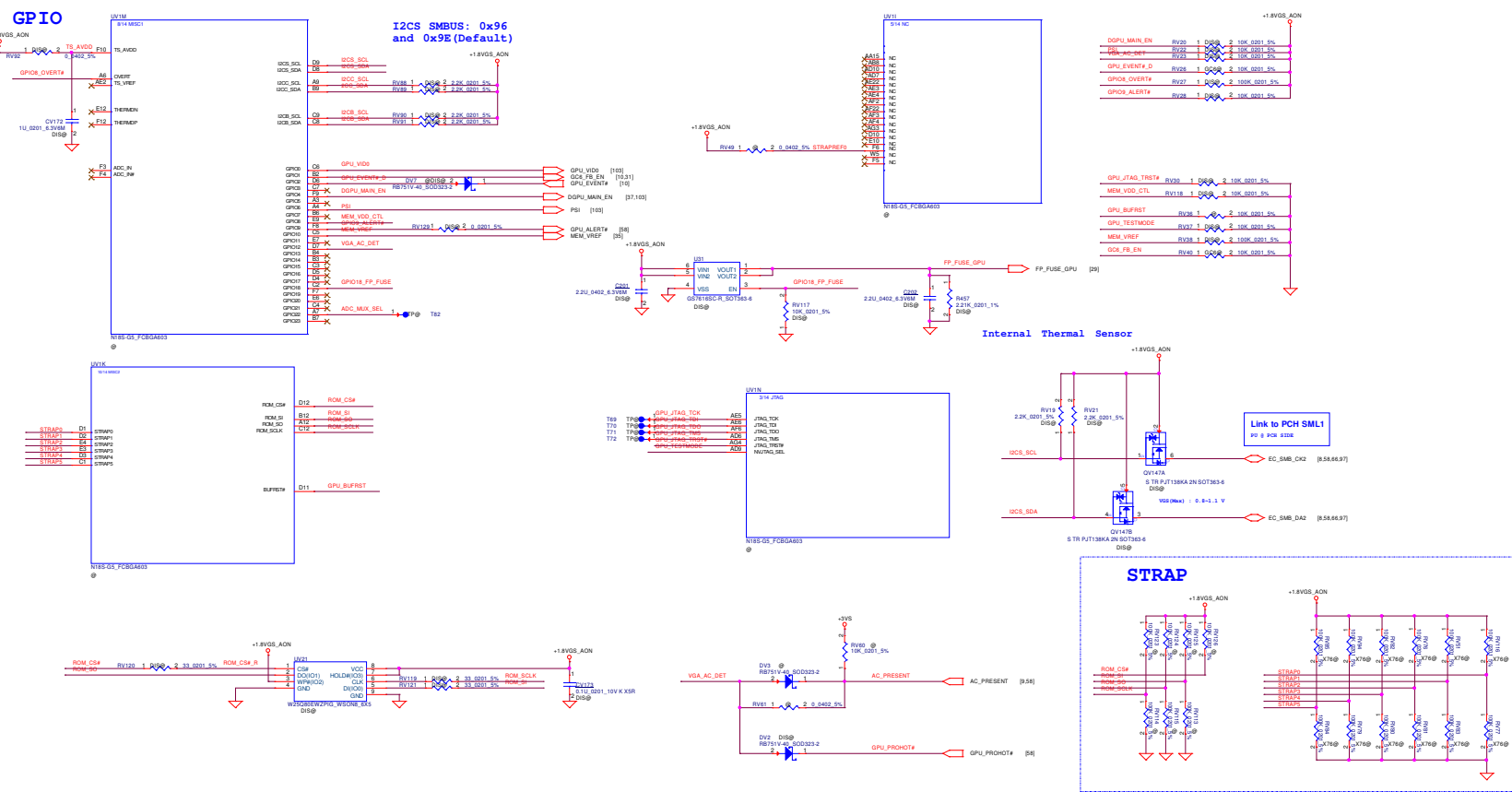
Table 3-17. PEX\_PLLVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 $\mu$ F	X7R	0402	1	Under GPU
1.0 $\mu$ F	X5R	0603	1	Near GPU
4.7 $\mu$ F	X5R	0805	1	Near GPU



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## N18S-G5 VRAM Strap

RAM_CFG	STRAP2	STRAP1	STRAP0	NOTE	Compal P/N
0x0 K4E80325BC-NC14	0	0	0	ZZZ V7E, V8D0@ X7000138058	SA0000C6260
0x1 MT61K256M32J-14:A	0	0	1	ZZZ N/A	
0x2 H56C8H24AIR-52C	0	1	0	ZZZ N/A	
0x5 H56G32C54DX005	1	0	1	ZZZ V7E, V8D0@ X7000138057	SA0000ENP00

Table 12. N18S-G5-B, N18S-G5, and N18S-LP GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940 <sup>2</sup>	Full	Production ready
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001 <sup>3</sup>	Full	Production ready
			Hynix	H56C8H24AIR-52C	A-die	0x2	14 Gbps	N/A	Full	Production ready
				H56G32C54DX005	C-die	0x5	16 Gbps	N/A	Full	Post-production ready

### Notes:

- For N18S-G5-B, N18S-G5 and N18S-LP, the maximum allowable memory case temperature is 95 °C.
- Before the date code is available, the specially screened Micron memory (for 11 Gbps @ 1.2V support) will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
- Before the date code is available, the specially screened Samsung memory (for 11 Gbps @ 1.2V support) is identified by "SPL" letters inserted before the seven digits in its lot ID.

## N18S Strap

	ROM_SI	ROM_SO	ROM_SCLK	STRAP3	STRAP4	STRAP5
Strap	RV113 S RES 1.20W 100K +5% 0201	RV115 S RES 1.20W 100K +5% 0201	RV114 S RES 1.20W 100K +5% 0201	RV116 S RES 1.20W 100K +5% 0201	RV117 S RES 1.20W 100K +5% 0201	RV118 S RES 1.20W 100K +5% 0201

Item	N18S-G5	MS-Hybrid Mode
Device ID	Primary: Secondary: N/A	
Package	GB2E-64	
Internal P/N		
ROM_SCLK (LSB)	1.80M Option for 100K PU to 1V8_AON 2.80M Option for 100K PD to GND	L
ROM_SI	1.80M Option for 100K PU to 1V8_AON 2.80M Option for 100K PD to GND	L
ROM_SO (MSB)	1.80M Option for 100K PU to 1V8_AON 2.80M Option for 100K PD to GND	L
Strap0 (LSB)	Refer to N18x_RAM_Straps table	
Strap1 (MSB)		
Strap2 (LSB)		
Strap3 (LSB)	1.80M Option for 100K PU to 1V8_AON 2.80M Option for 100K PD to GND	L
Strap4	1.80M Option for 100K PU to 1V8_AON 2.80M Option for 100K PD to GND	L
Strap5 (MSB)	1.80M Option for 100K PU to 1V8_AON 2.80M Option for 100K PD to GND	L
Boot Voltage	0.8V	

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				LA-M062P
				Rev
				0.1







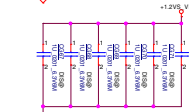
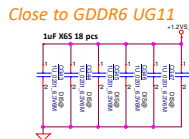
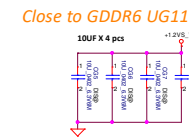
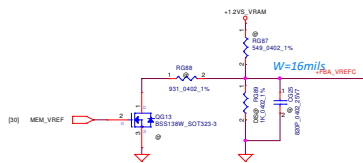
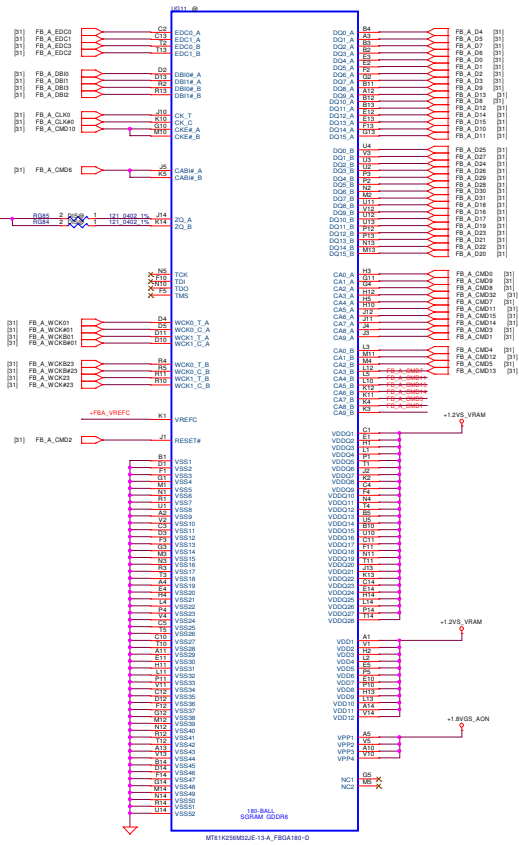
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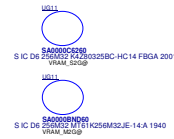
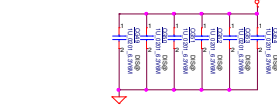
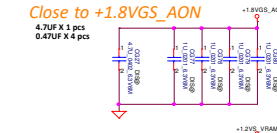
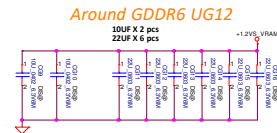
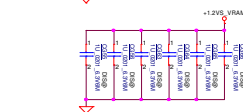
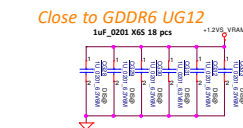
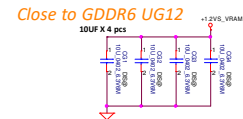
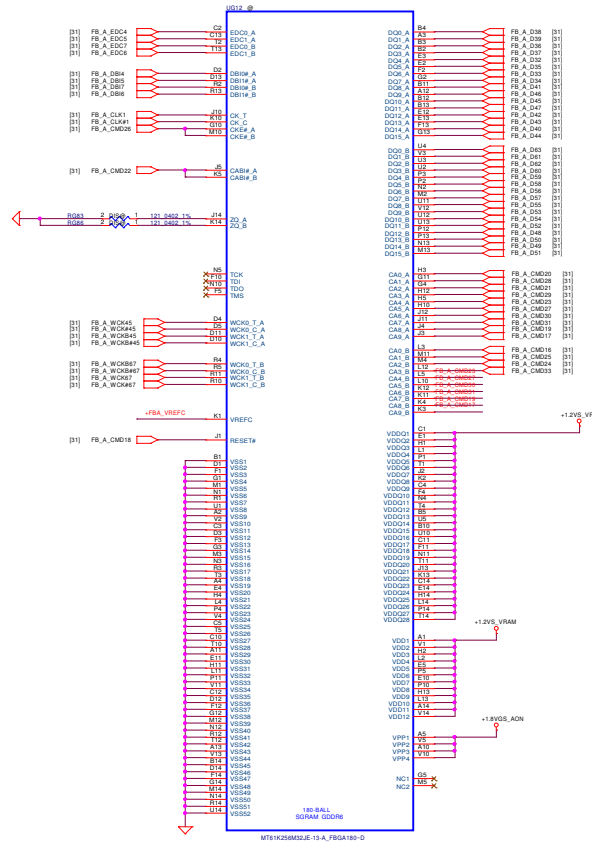
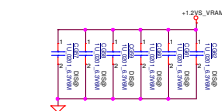
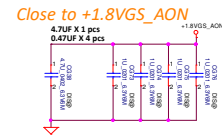
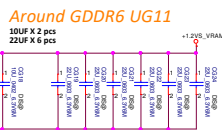
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## VRAM A

DCORE Job Mapping		4.0 Nodes
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CMB, A	CMB6	CMB6
CMB, A	CMB7	CMB7
CMB, A	CMB8	CMB8
CMB, A	CMB9	CMB9
CMB, A	CMB10	CMB10
CMB, A	CMB11	CMB11
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0825 update P/N

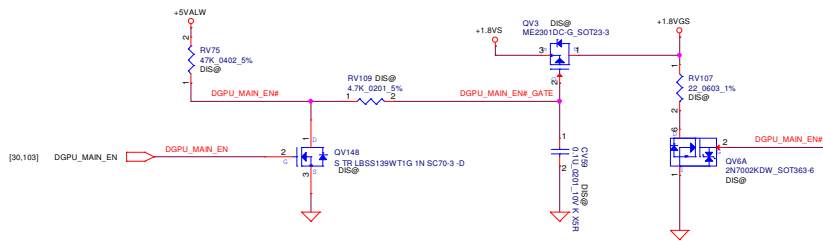


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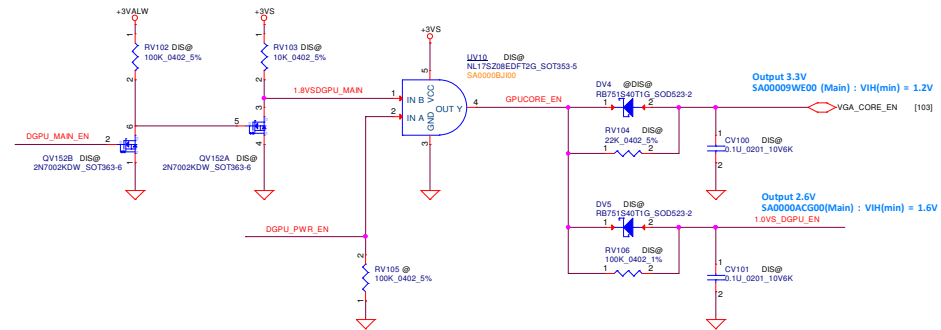
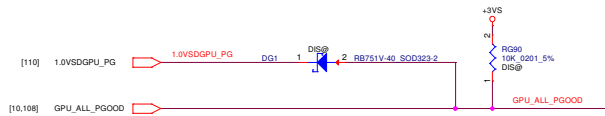
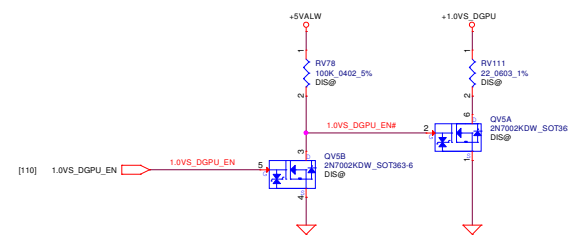
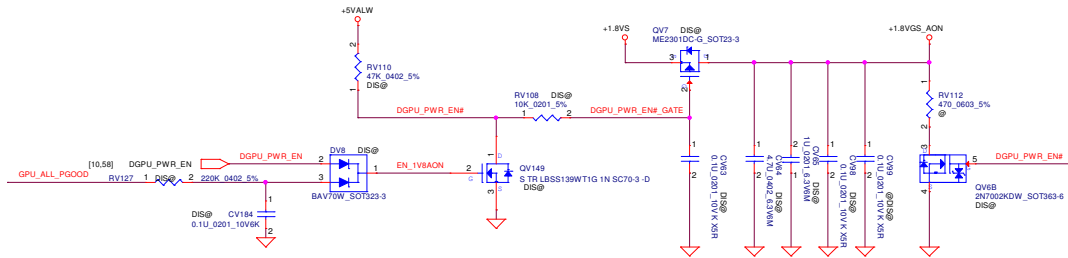


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### +1.8VS to +1.8VGS



### +1.8VS to +1.8VGS\_AON



### 7.3.2.1 Power-Up Sequence

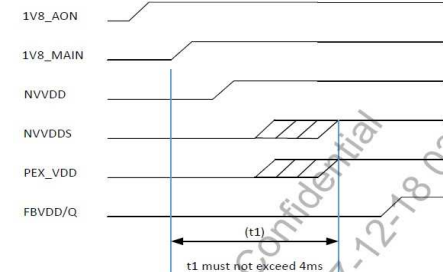
The following power-up sequence is required:

1V8\_AON → 1V8\_MAIN → NVVDD → NVVDDS / PEX\_DVDD → FBVDD(Q)

► All GPU power rails must ramp up after 1V8\_AON.

► FBVDD(Q) should ramp up after NVVDDS and PEX\_DVDD.

All other 1.8V power rails can ramp up with 1V8\_MAIN including PEX\_HVDD and all PLLVDD rails; all other 1V power rails can ramp up with PEX\_DVDD.



### 7.3.2.2 Power-Down Sequence

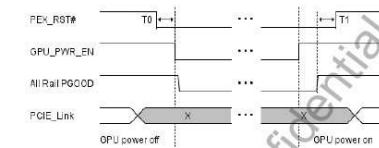
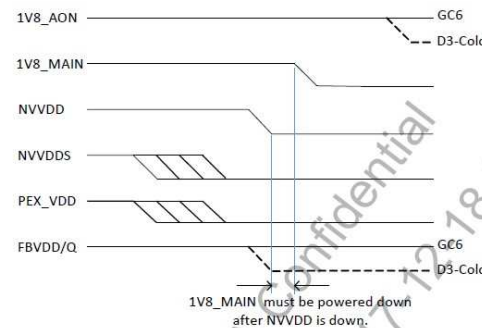
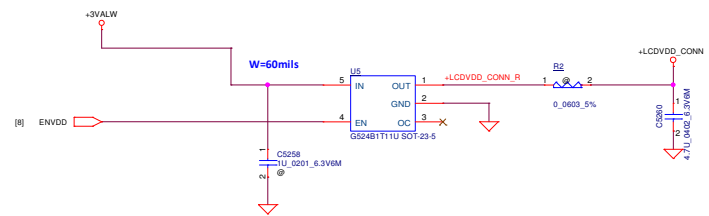


Figure 8.9 GC OFF Entry/Exit Timing Diagram

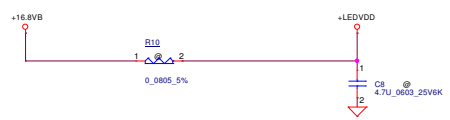
Table 8.1 GC OFF Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

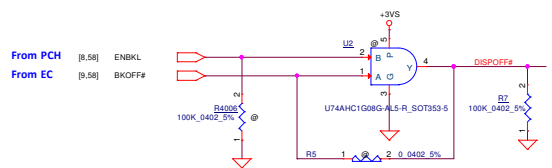
LCD POWER SWITCH



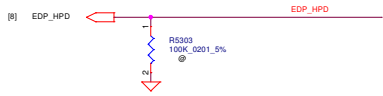
LED POWER



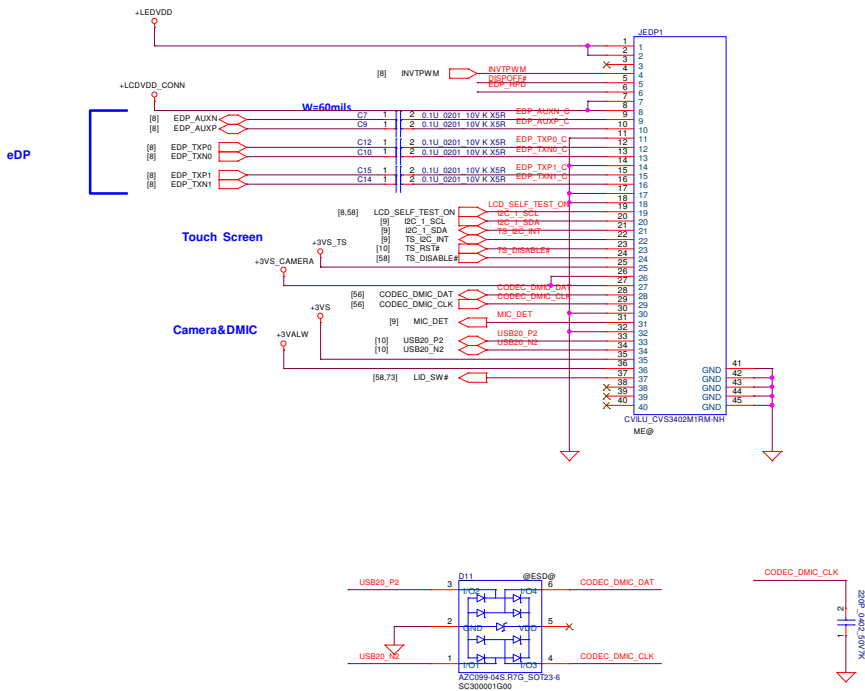
DISPLAY OFF



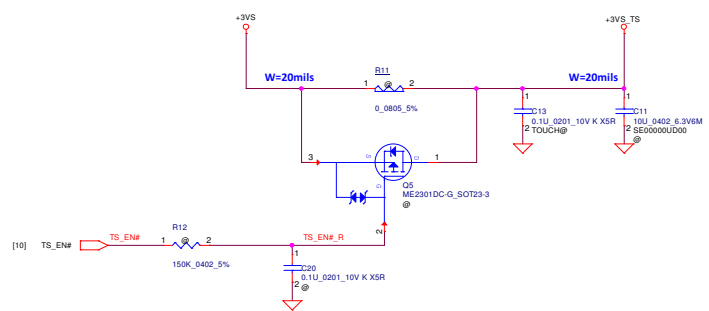
HOT PLUG DETECT



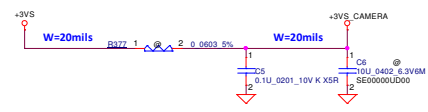
eDP CONNECTOR



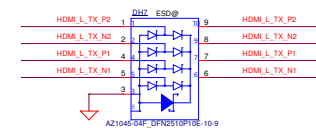
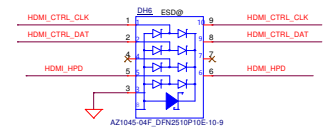
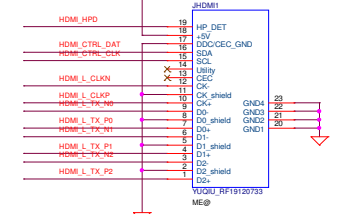
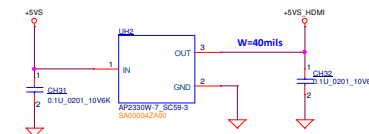
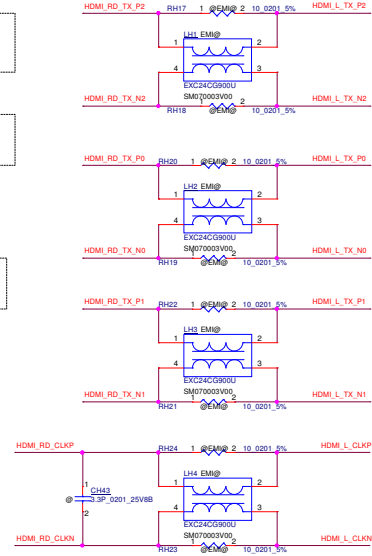
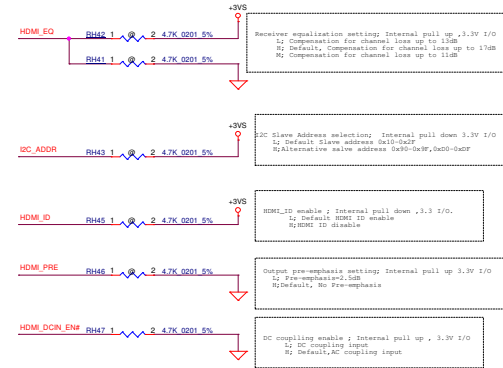
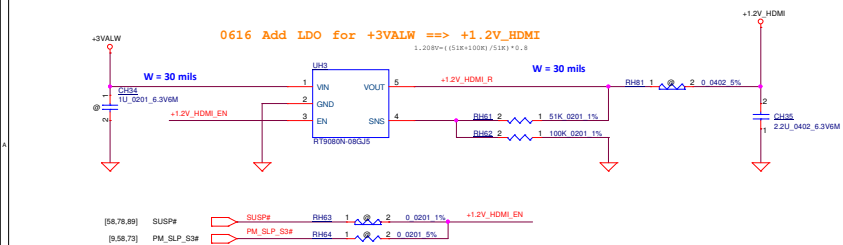
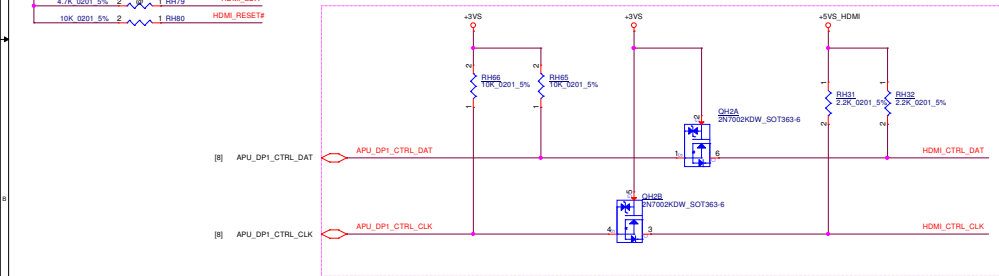
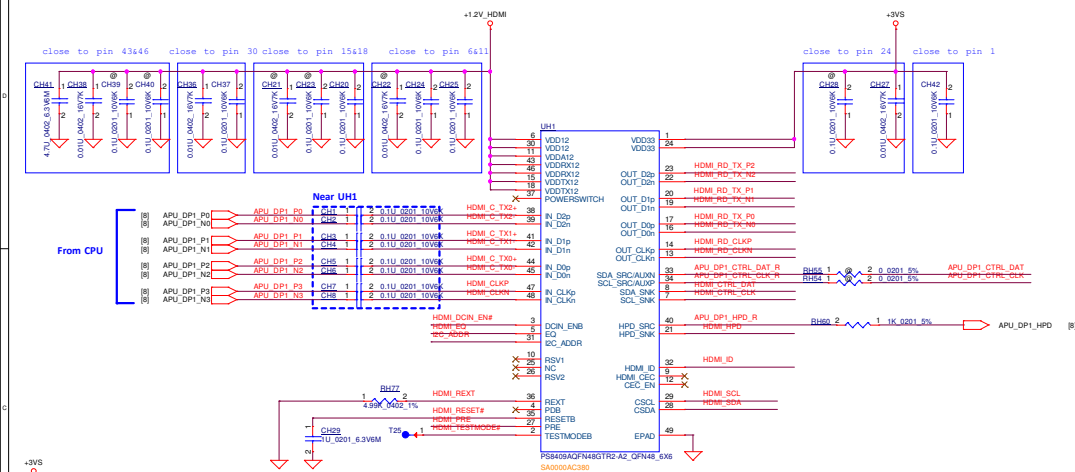
Touch Screen POWER CIRCUIT



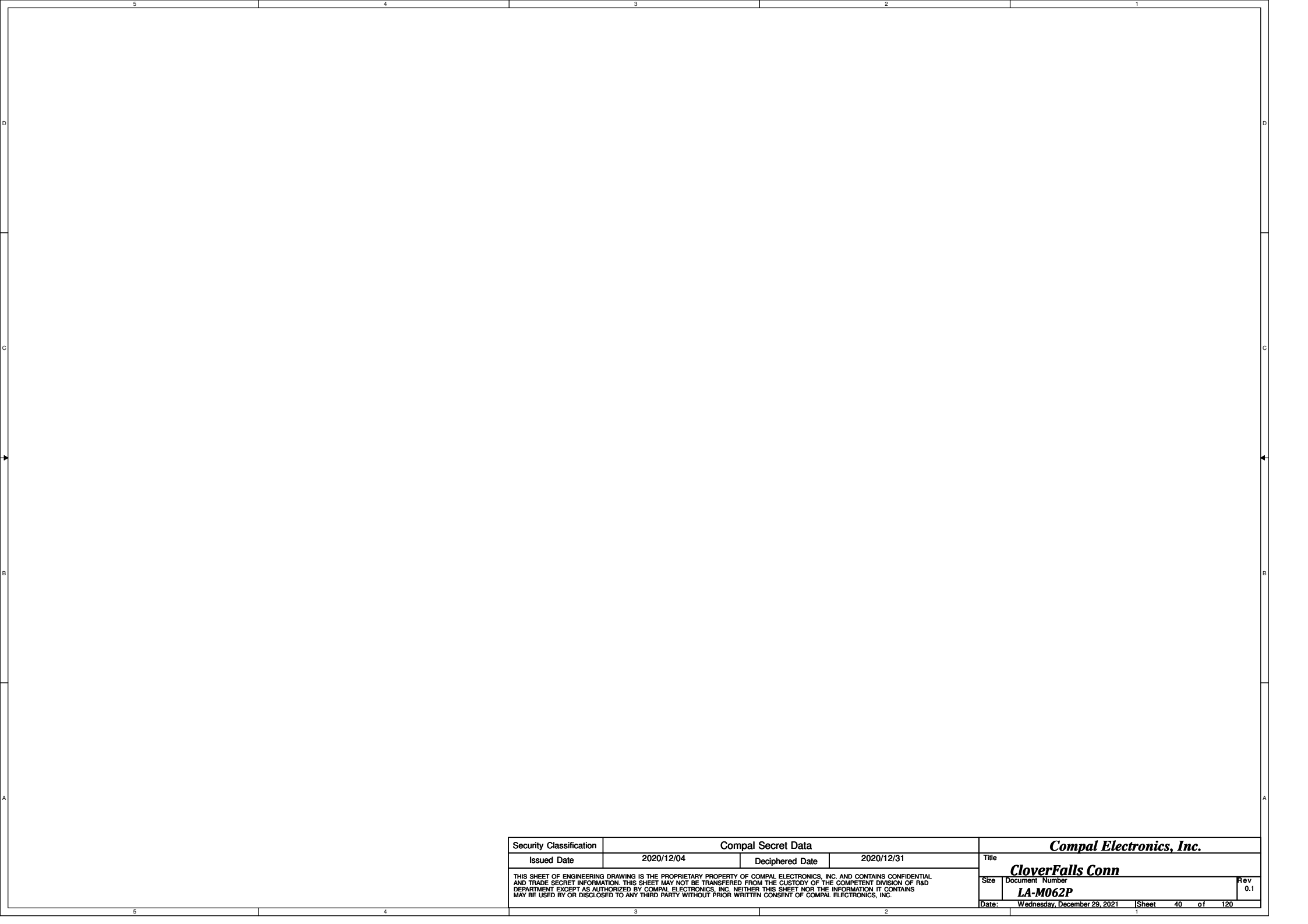
CAMERA POWER CIRCUIT



# HDMI 2.0\_PS8409A



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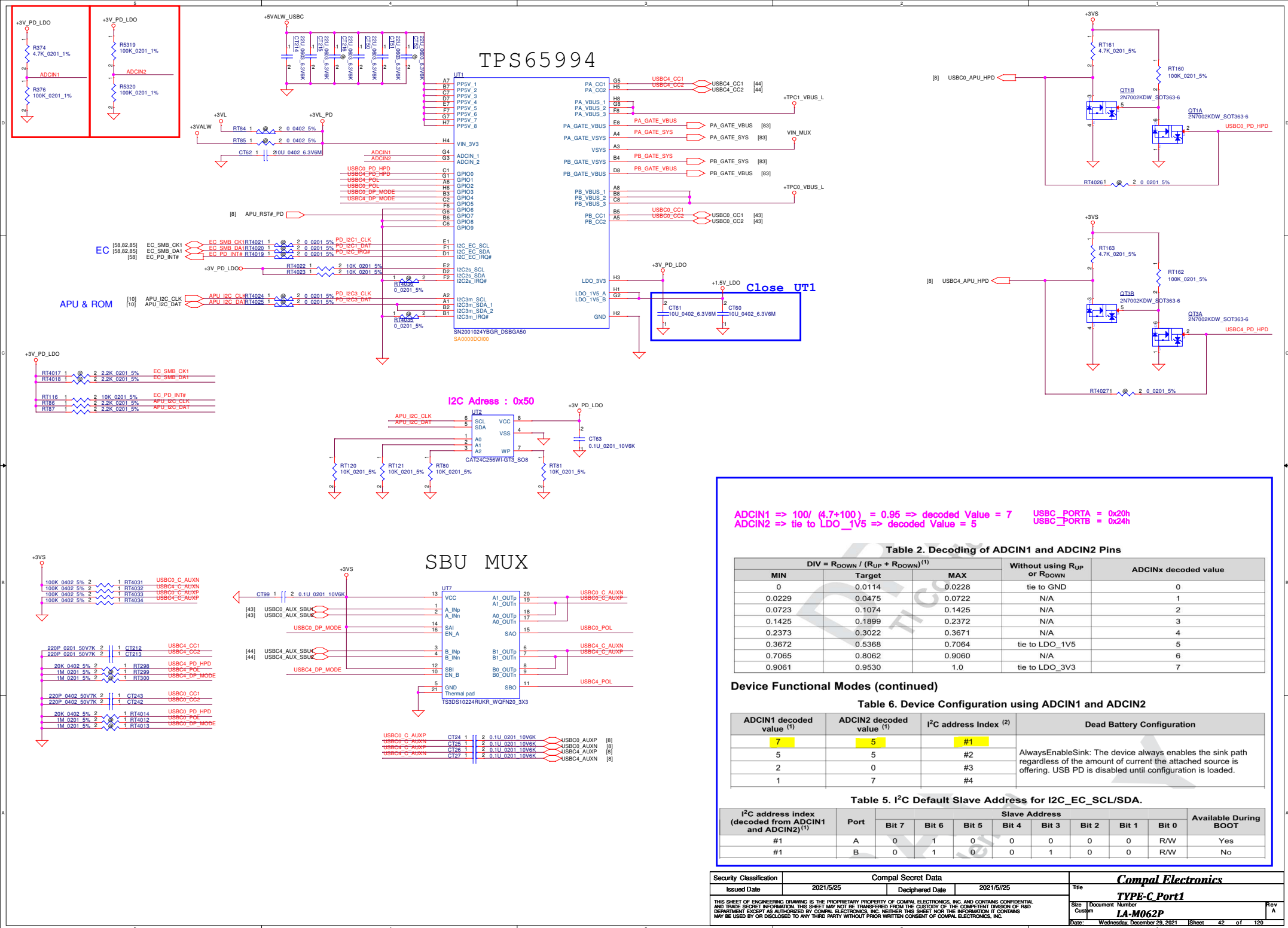


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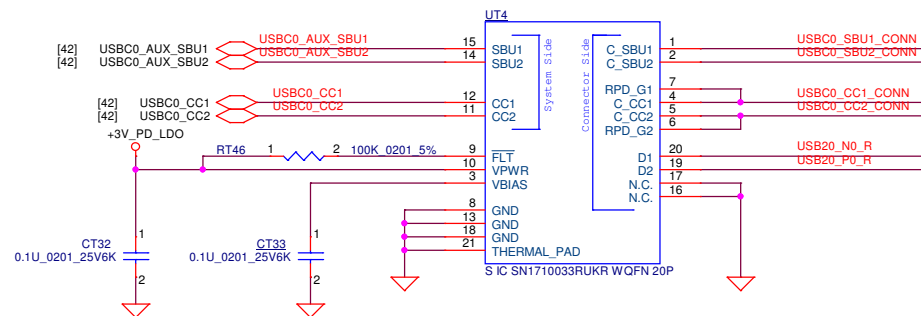
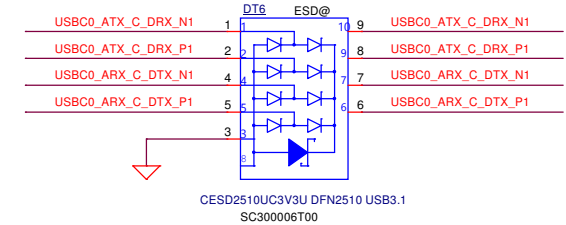
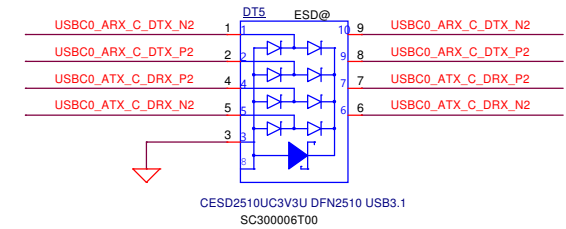
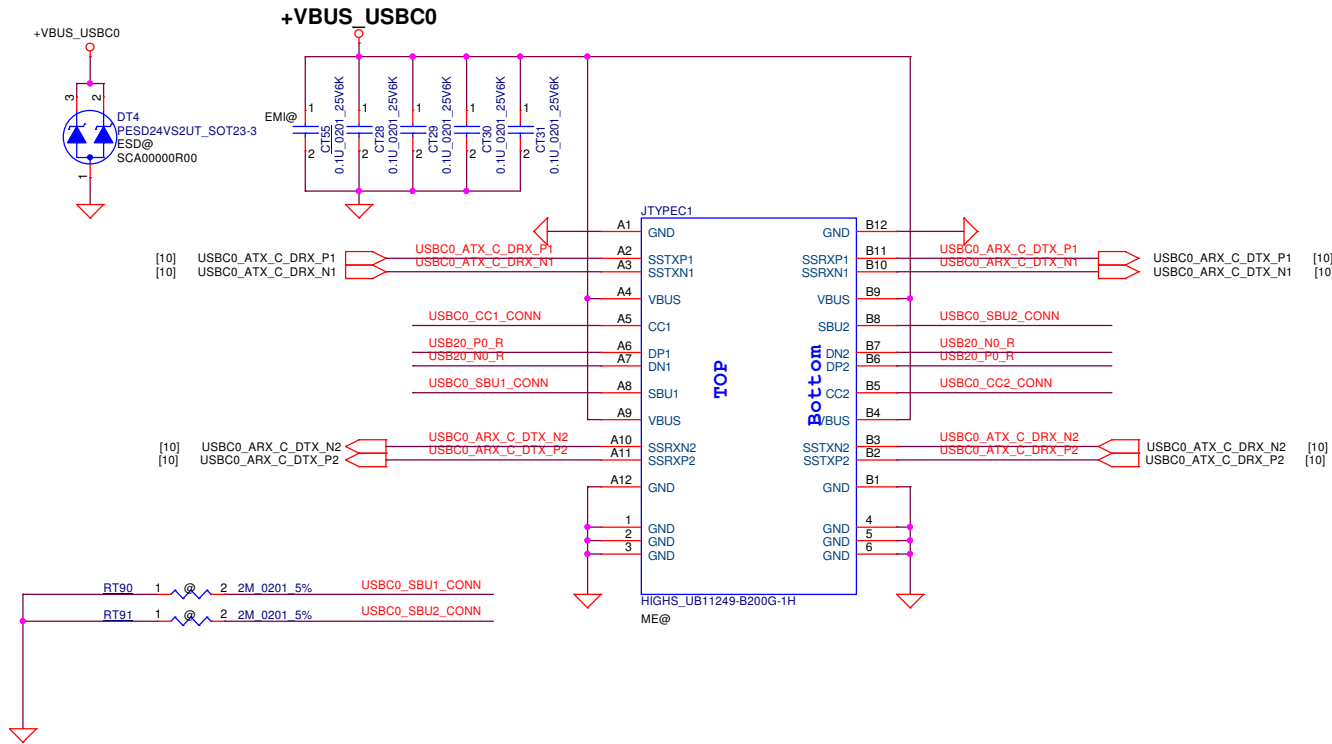
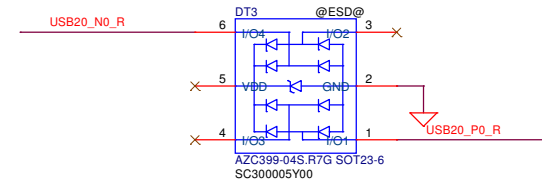
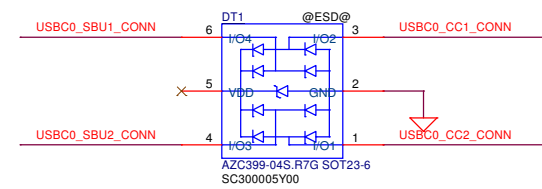
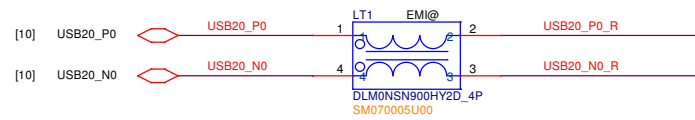




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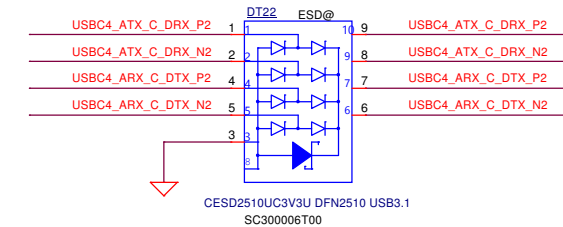
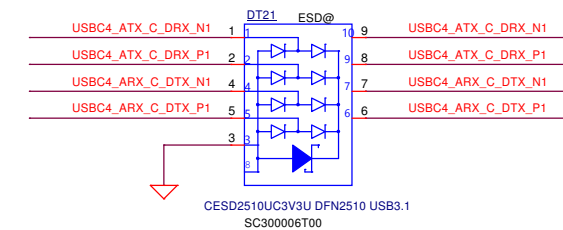
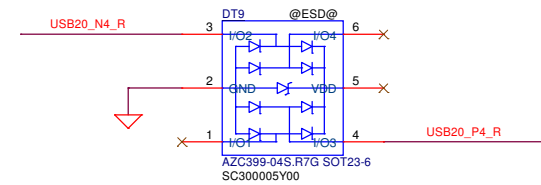
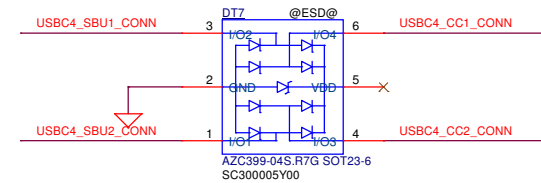
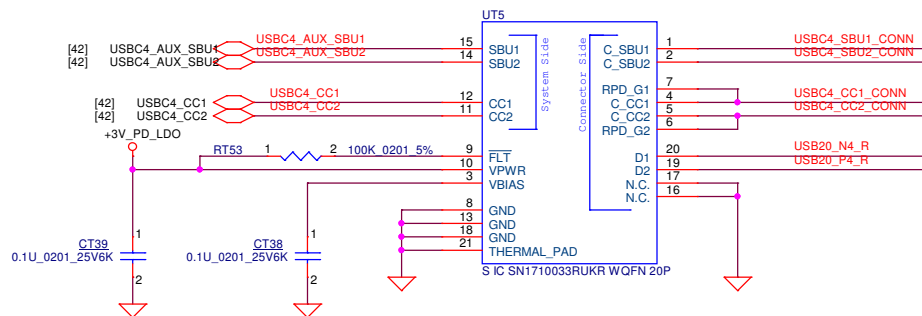
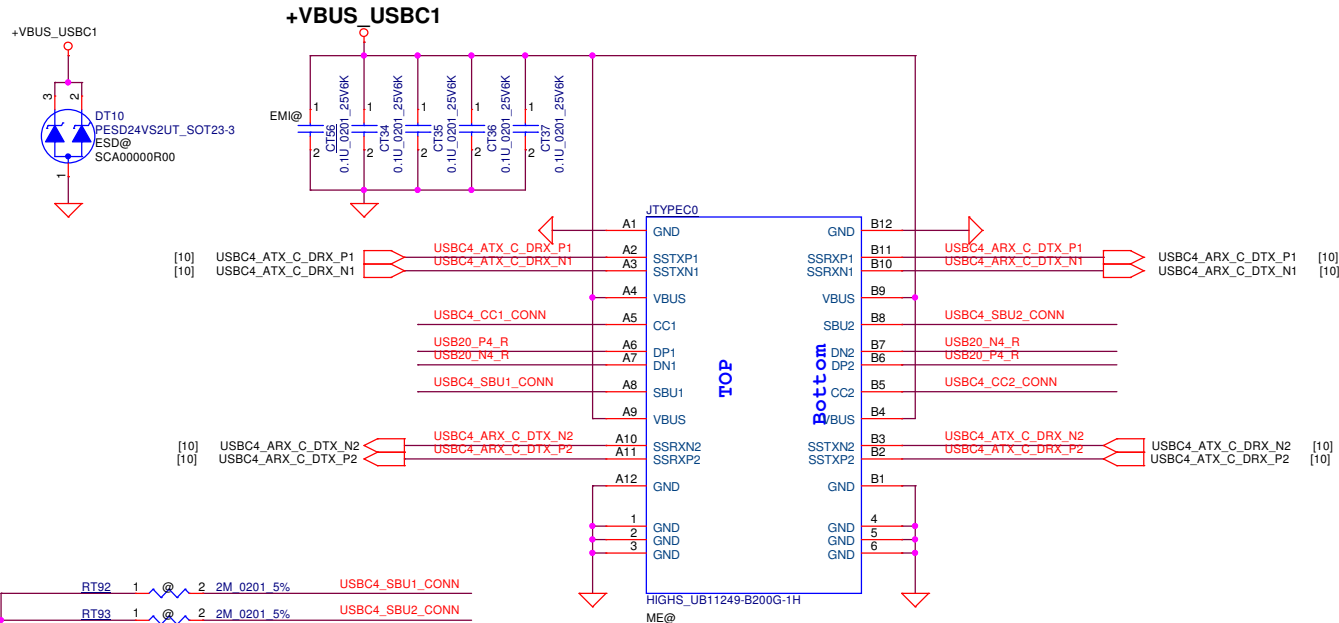
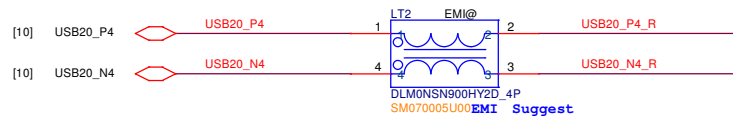


## TYPE-C PORT1



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## TYPE-C PORT2



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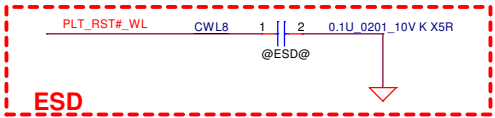
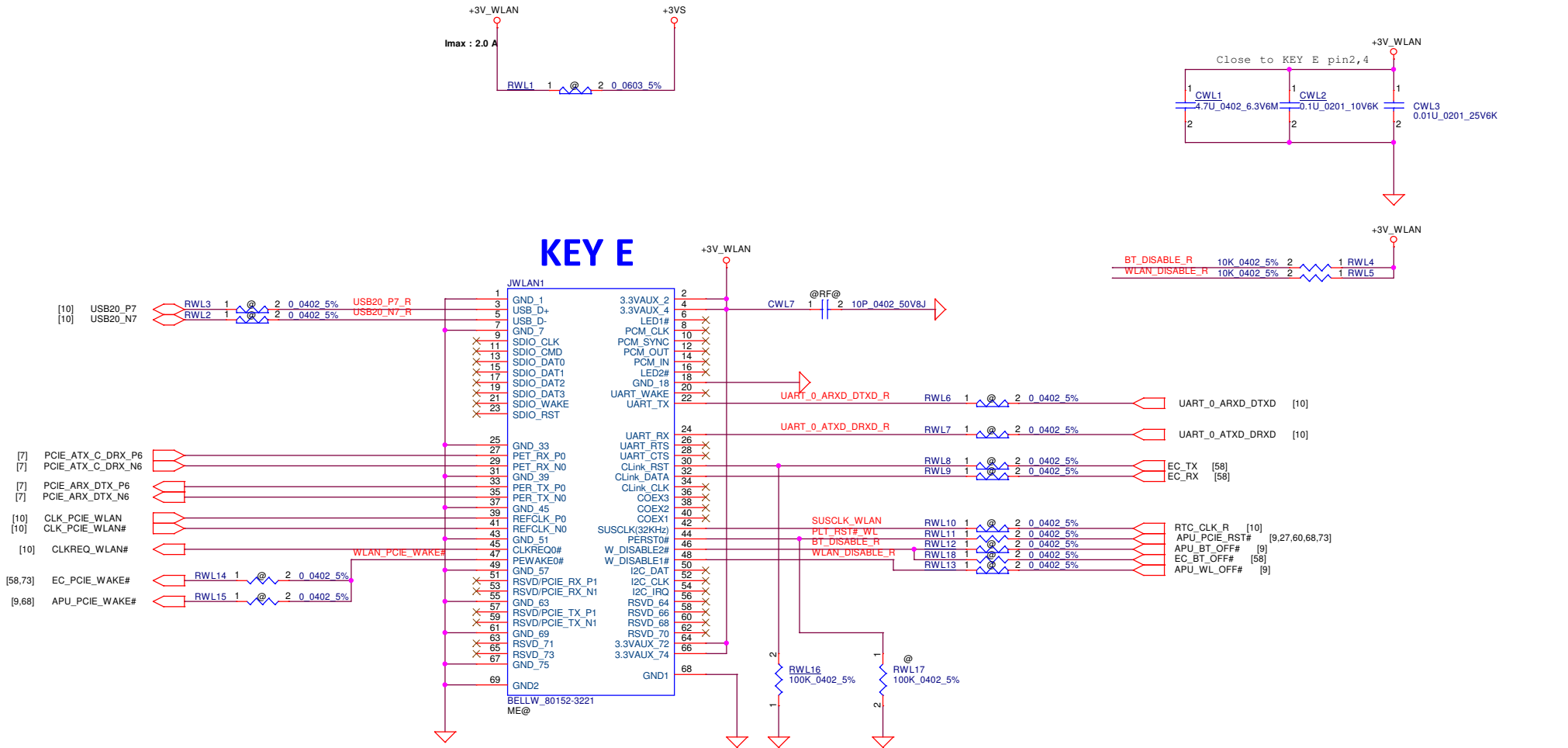


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WLAN(TYPE E)



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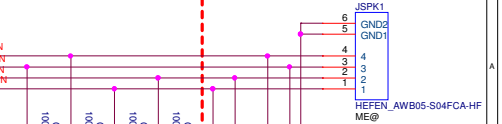
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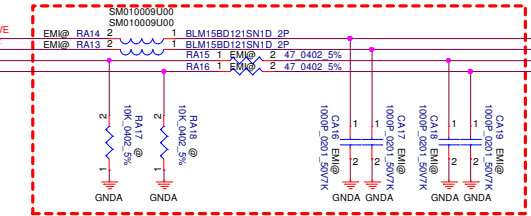
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SPEAK 4 ohm : 40MIL  
SPEAK 8 ohm : 20MIL

SPK\_L1- RA5 1 @ 2 0.0603 5% SPK\_L1- CONN  
SPK\_L2+ RA6 1 @ 2 0.0603 5% SPK\_L2+ CONN  
SPK\_R1- RA1 1 @ 2 0.0603 5% SPK\_R1- CONN  
SPK\_R2+ RA3 1 @ 2 0.0603 5% SPK\_R2+ CONN

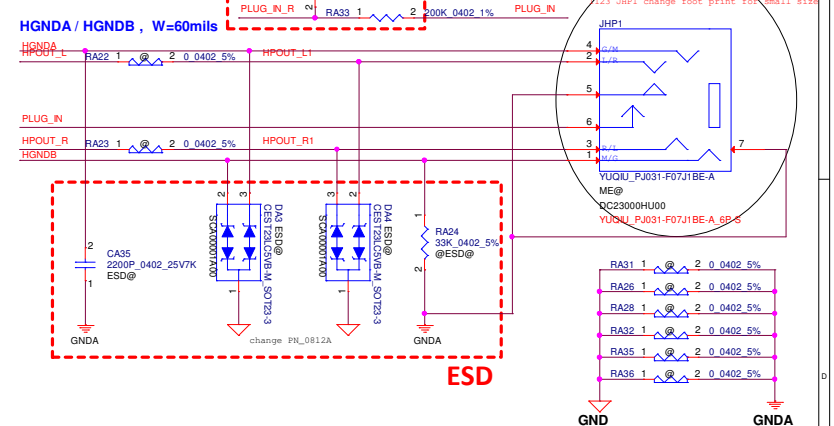


W=40mils  
W=40mils

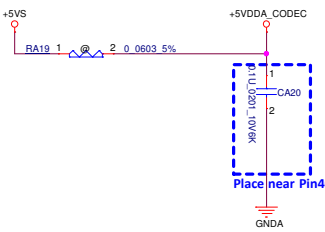


Close Audio codec

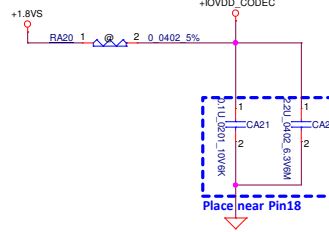
Combo Jack  
(Normal Open)



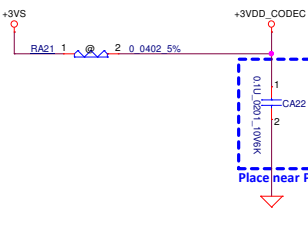
+5VS --&gt; +5VDDA\_CODEC



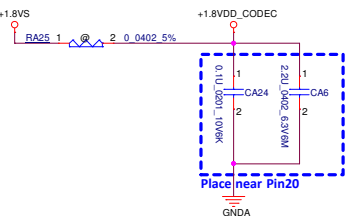
+1.8VS --&gt; +1.8VDD\_CODEC



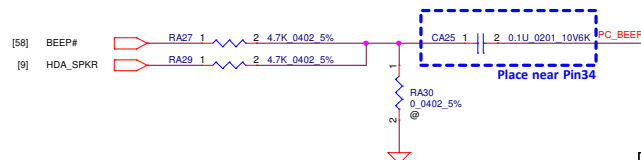
+3VS --&gt; +3VDD\_CODEC



+1.8VS --&gt; +1.8VDD\_CODEC



PC Beep

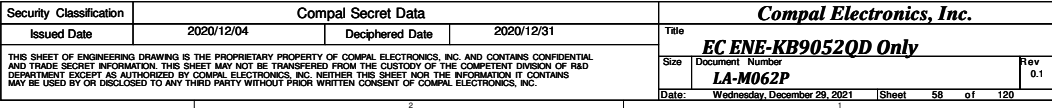


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				Date:	Wednesday, December 29, 2021
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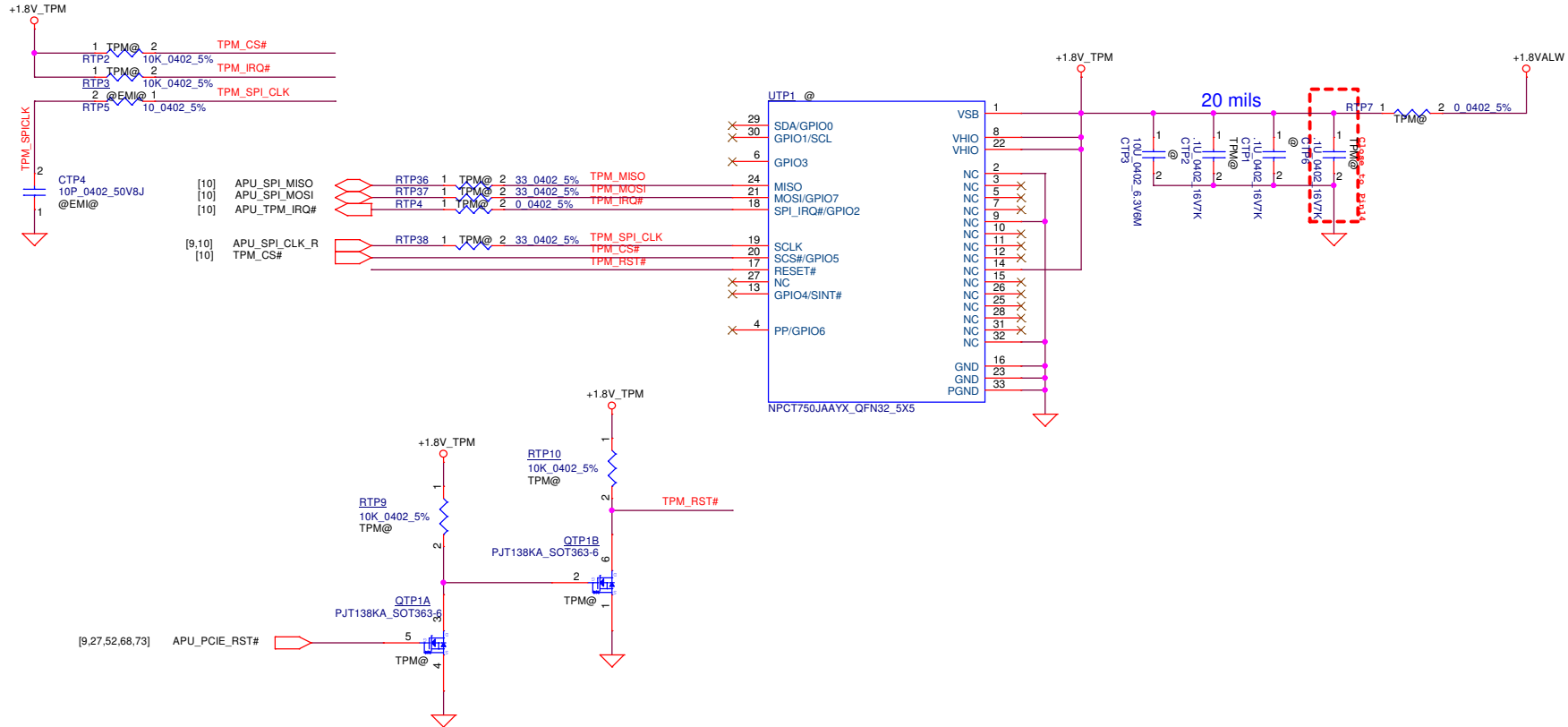
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Date: Wednesday, December 29, 2021	Rev 0.1
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# TPM/TCM IC

## TPM 2.0 Co-layer

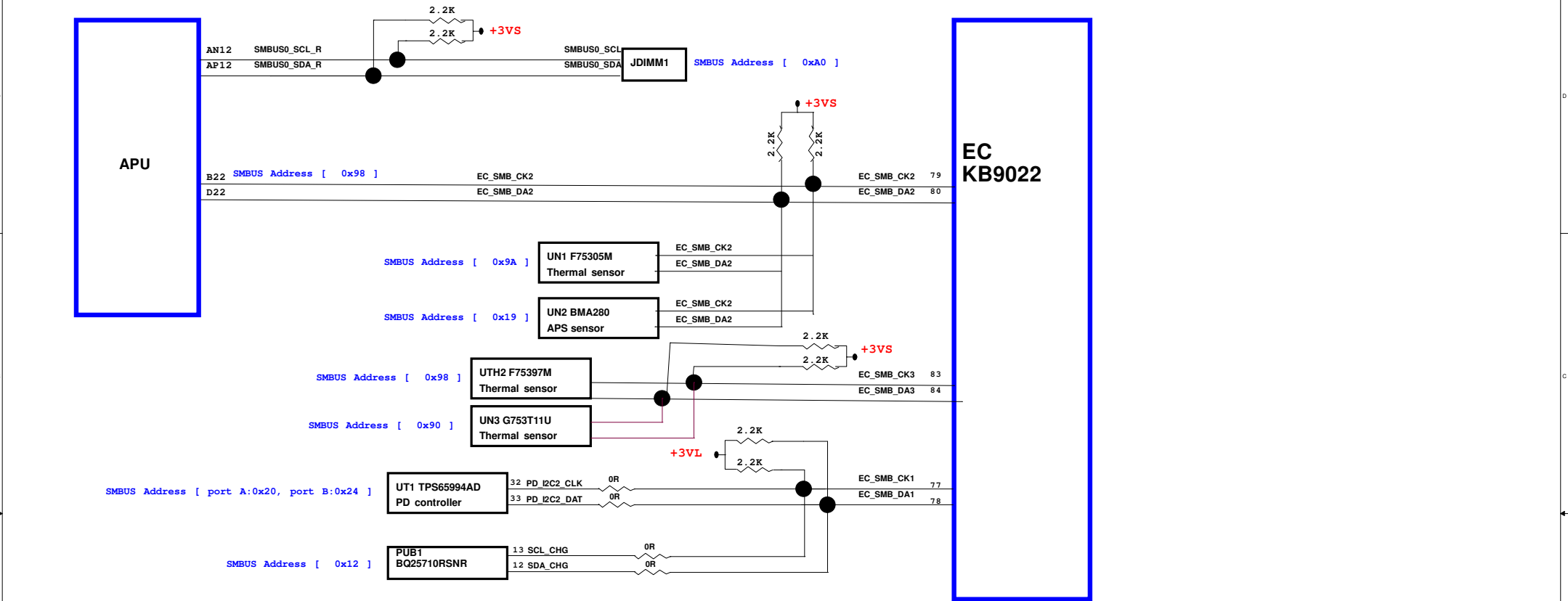
- 1.Nuvton\_NPCT750LABYX
- 2.ST\_ST33HTPH2E32AAE8
- 3.Nations\_Z32H330TC

UTP1 Nuvton@ SA0000EO000 S IC NPCT760LAAAYX QFN 32P TPM  
 UTP1 Nations@ SA0000ASZ30 S IC Z32H330TC-SQN-L4 QFN 32P TPM  
 UTP1 ST@ SA0000CY050 IC ST33HTPH2X32AEH0 VFQFPN 32P TPM

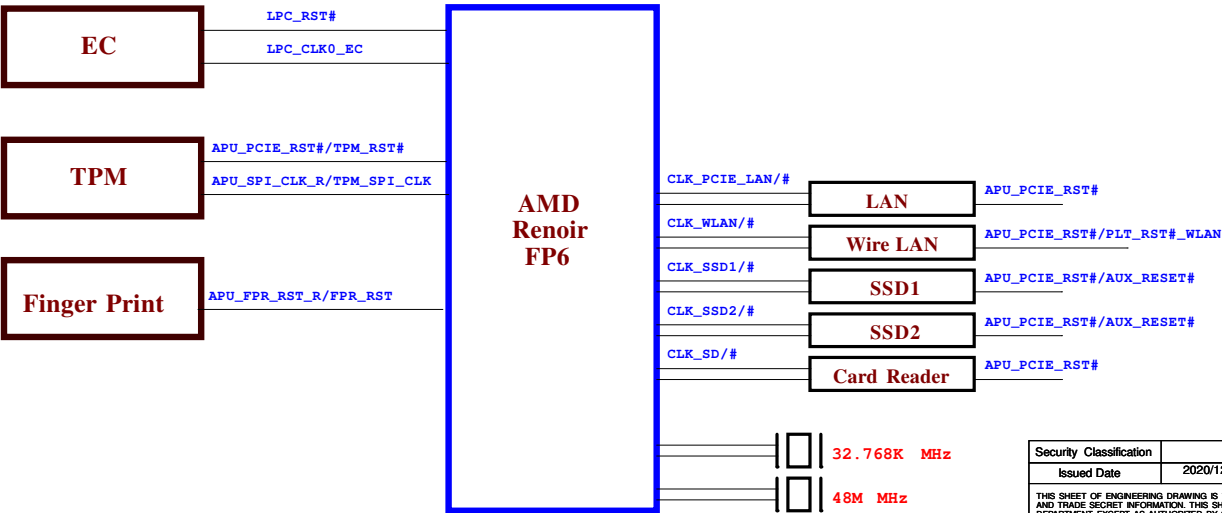


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Size	Document	Number	Rev	LA-M062P	
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# SMBus Block Diagram



## System clock and Reset map

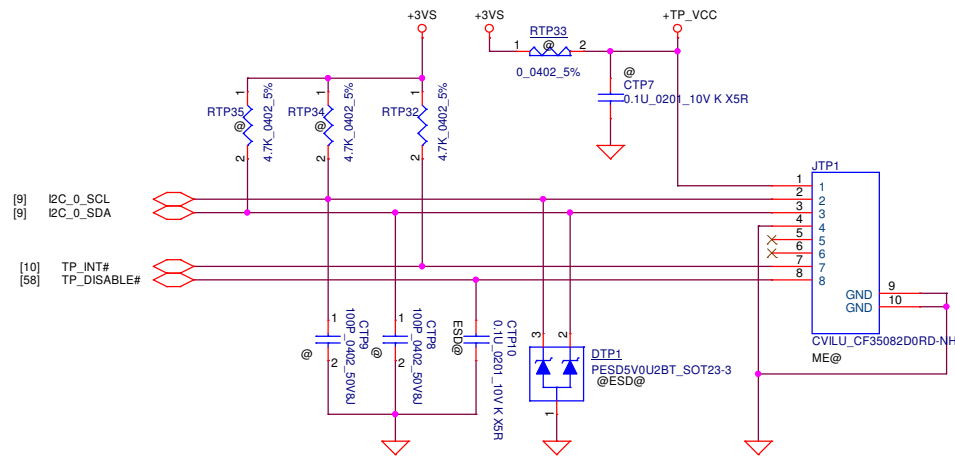


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				Custom	LA-M062P	0.1
				Date:	Wednesday, December 29, 2021	Sheet 61 of 120

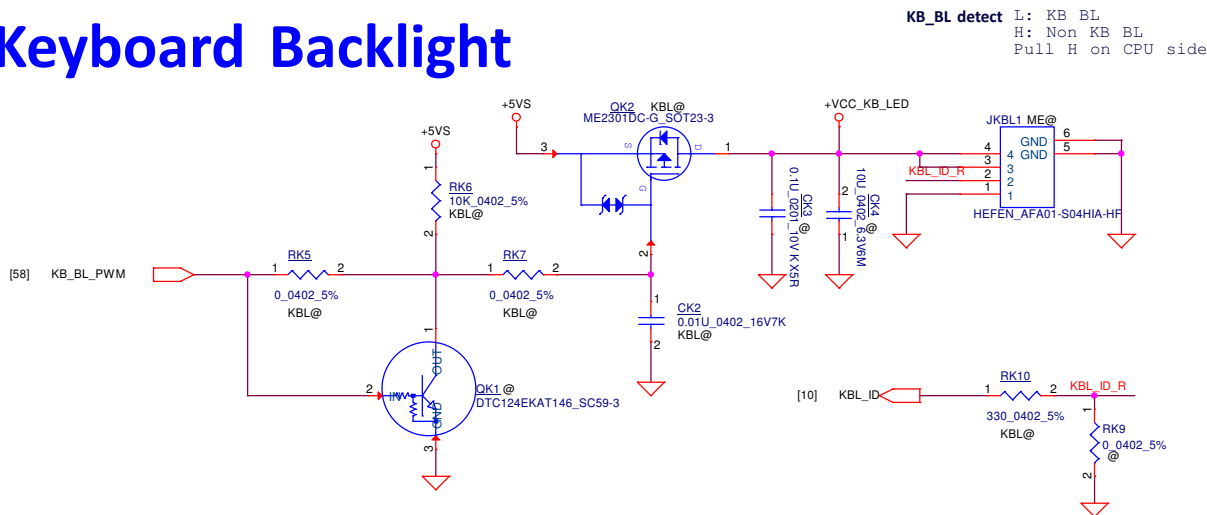


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				Size	Document Number
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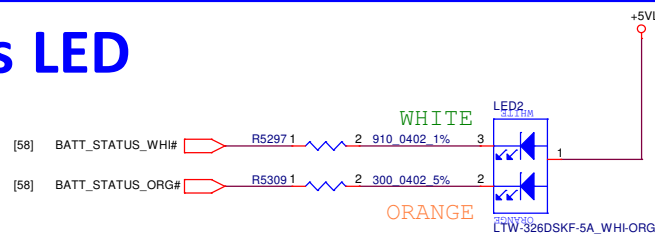
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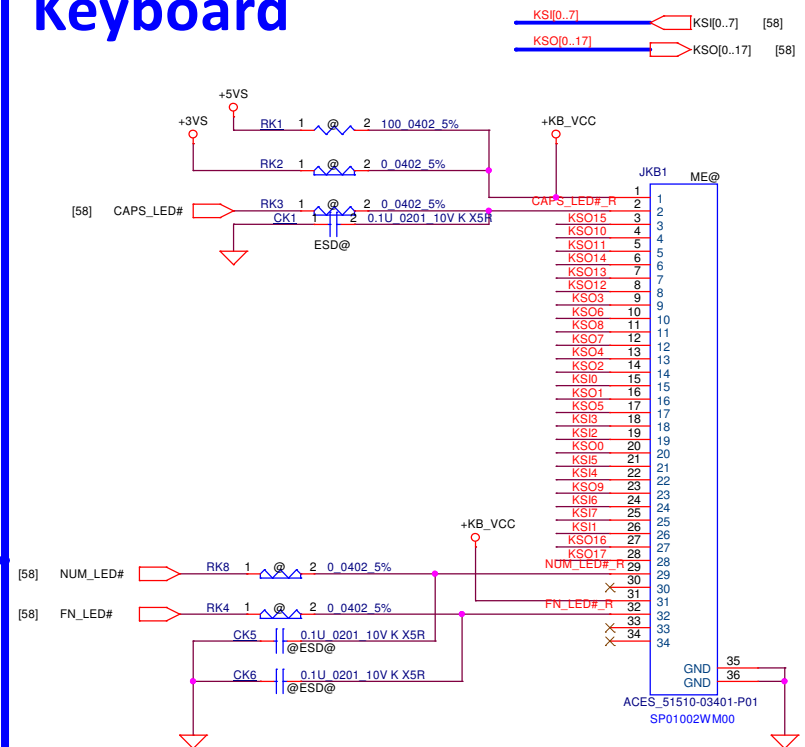
# Keyboard Backlight



# Status LED

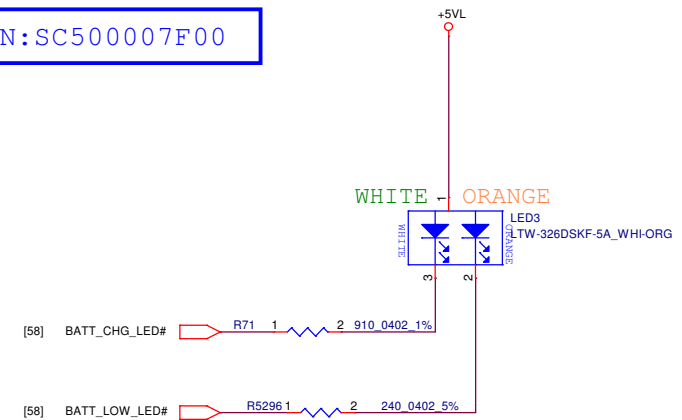


# Keyboard



# Charge LED

P/N:SC500007F00



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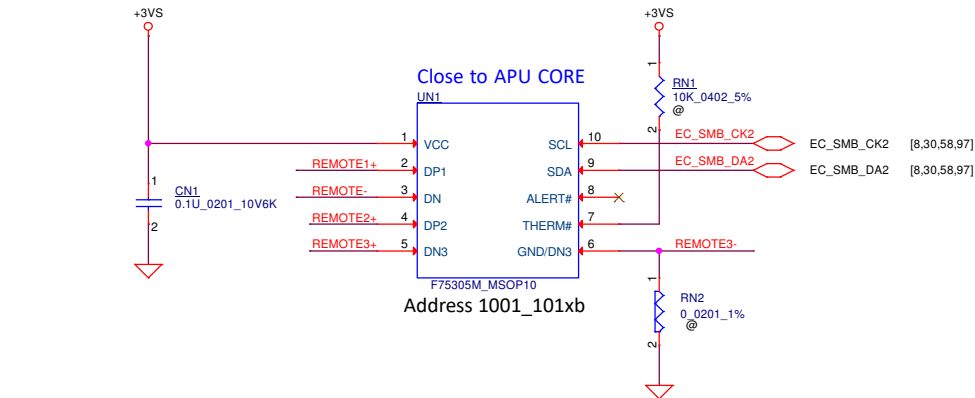
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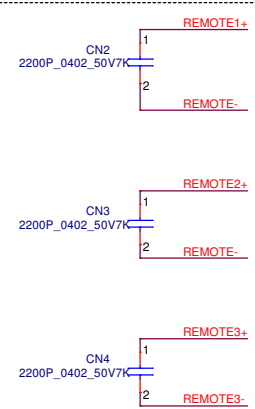
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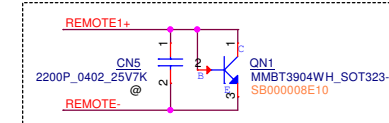
## Thermal Sensor



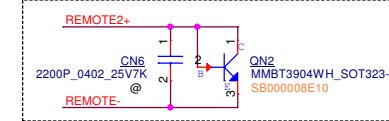
### Close to UN1



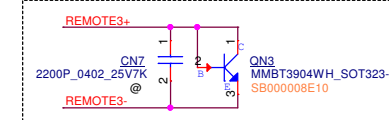
### Close to BATT Charger (JBATT1)



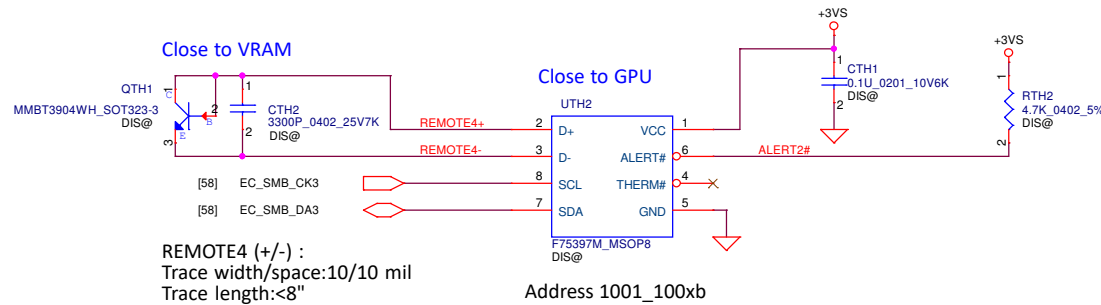
### Close to SSD



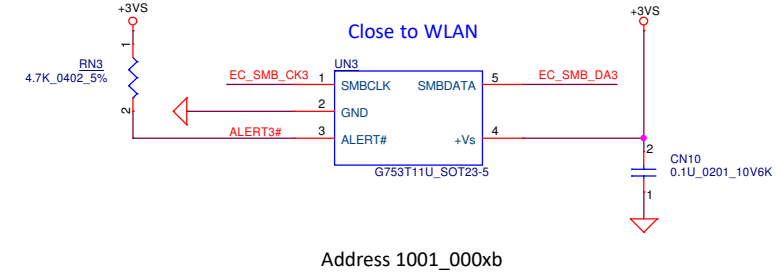
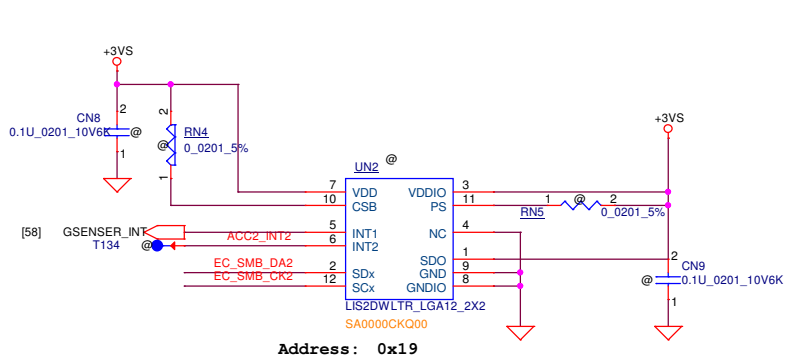
### Close to WLAN (JWLAN1)



REMOTE1,2,3 (+/-) :  
Trace width/space:10/10 mil  
Trace length:<8"



## Intelligent Cooling G-Sensor

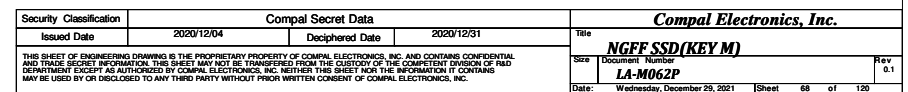


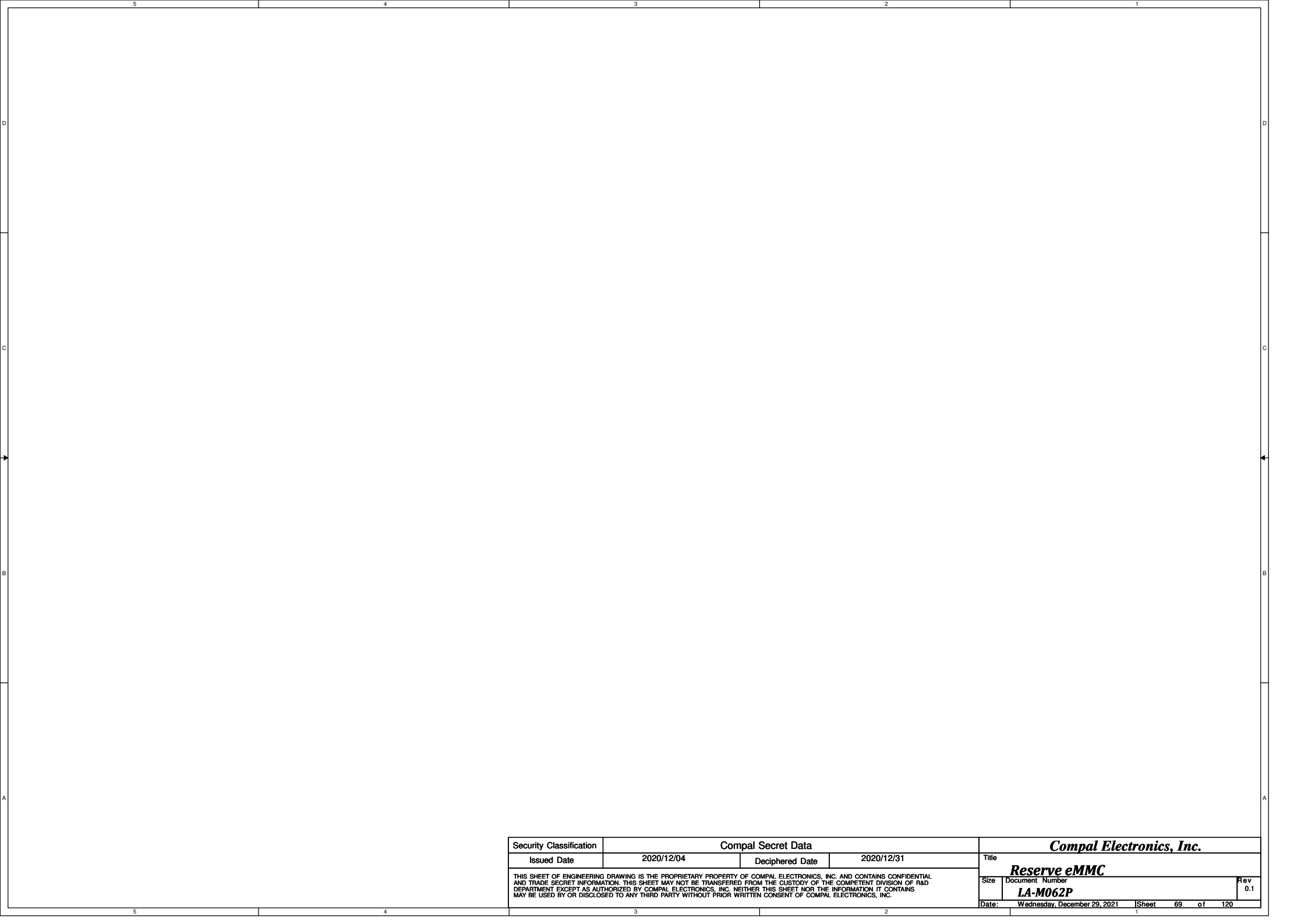
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1	2	3	4	5
D				D
C				C
B				B
A				A
1	2	3	4	5

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					<b>LA-M062P</b>
Date: Wednesday, December 29, 2021				Sheet	67 of 120
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## 2nd SSD(TYPE M)

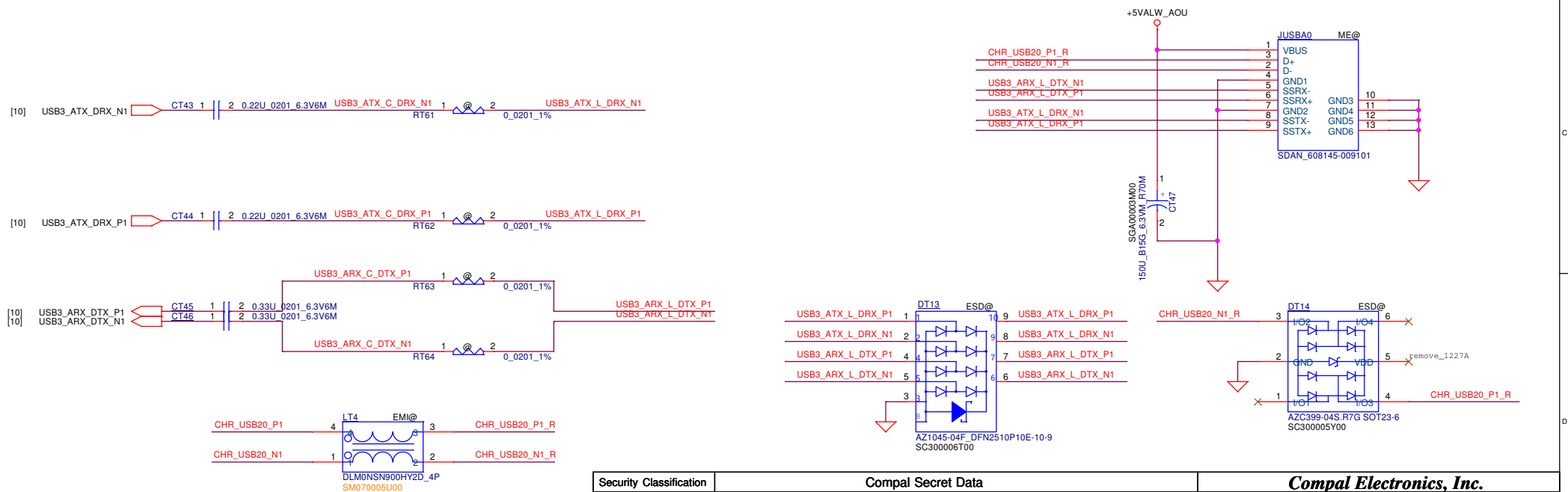
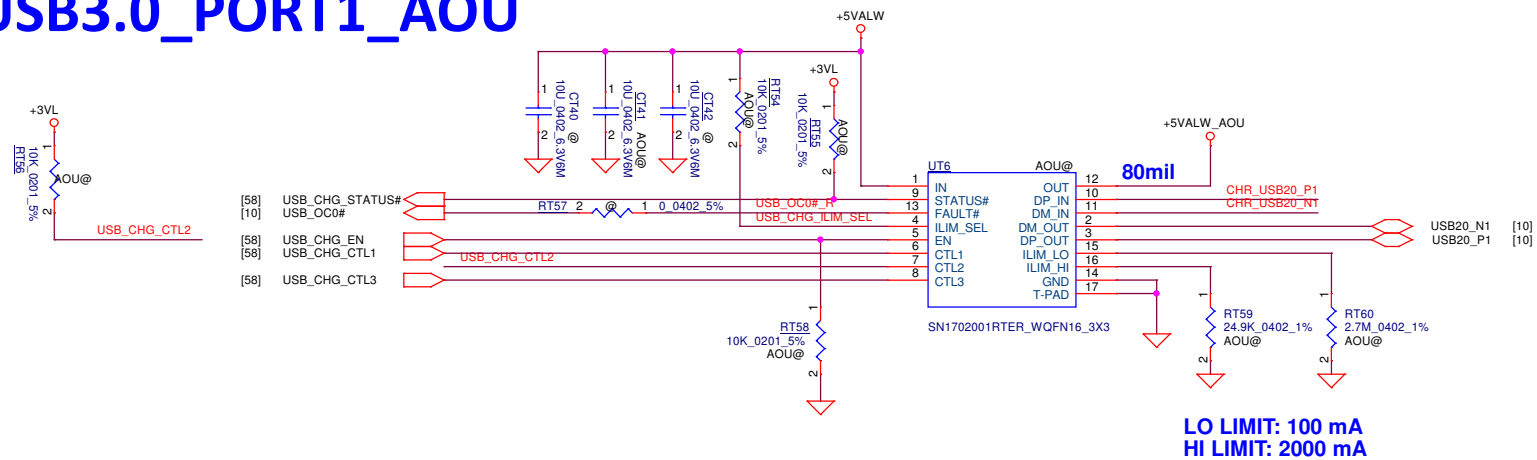




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# USB3.0\_PORT1\_AOU



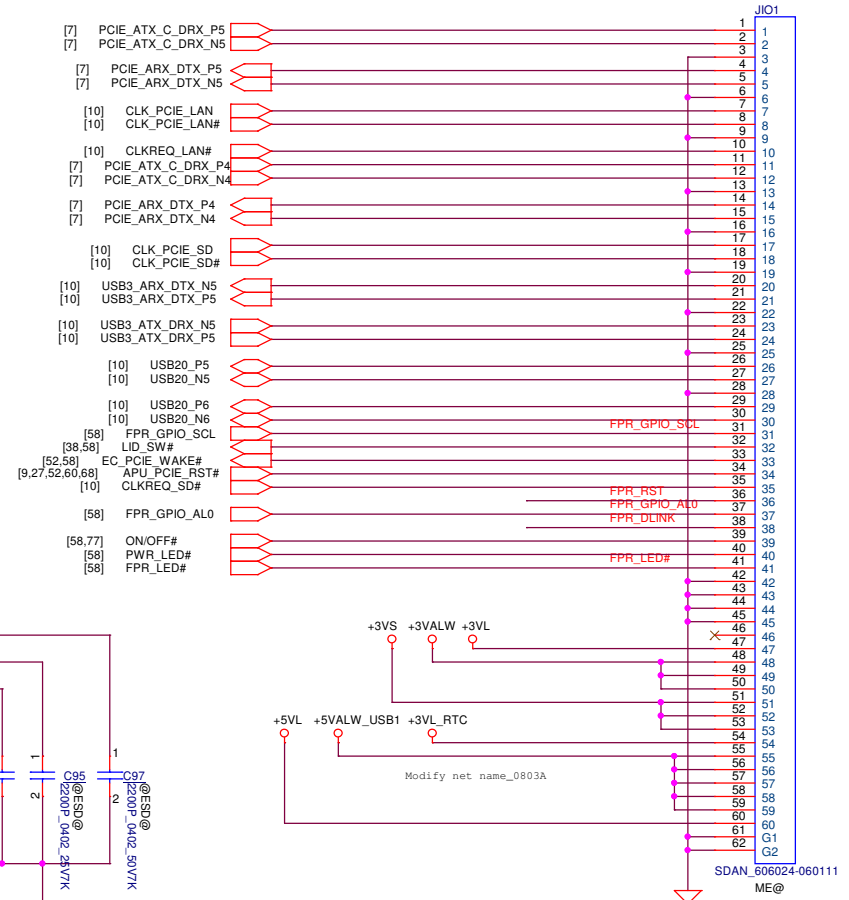
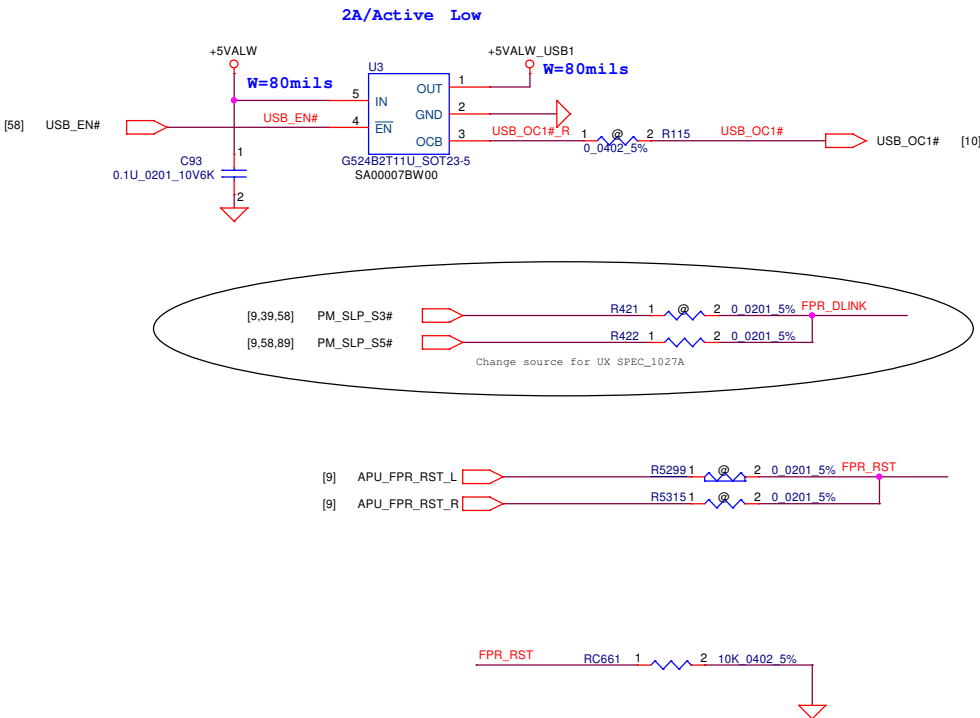
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Issued Date	2020/12/04	Deciphered Date	2020/12/31	Title		
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## USB3.0 SW to IO/B



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				Date:	Wednesday, December 29, 2021	Sheet 73 of 120



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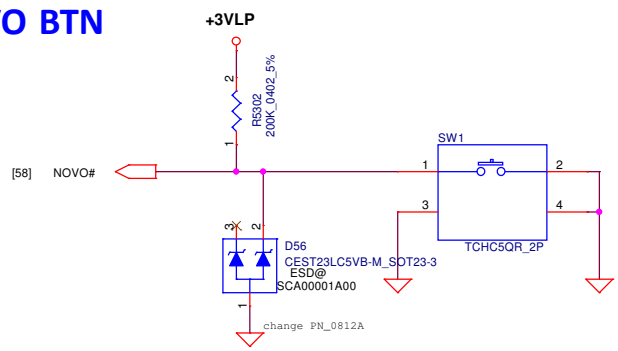
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				Date:	Wednesday, December 29, 2021
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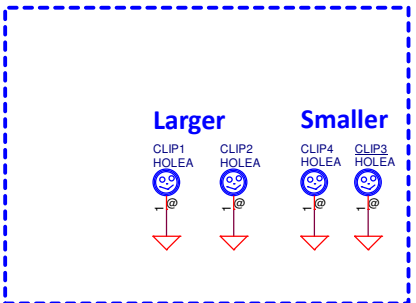


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				Size	Document Number
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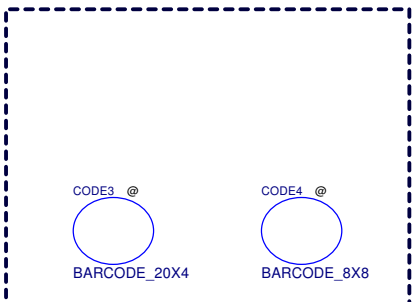
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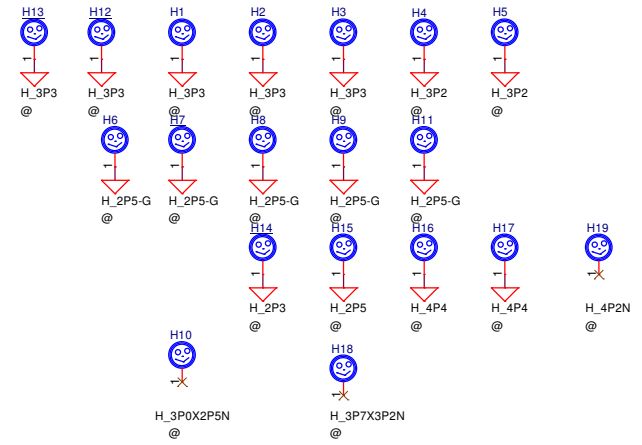
Shielding Clip



LASER BARCODE



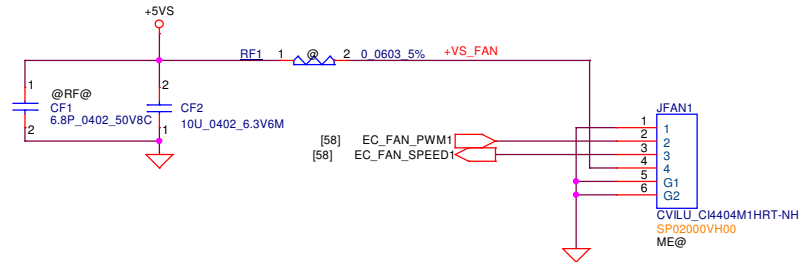
Screw Hole



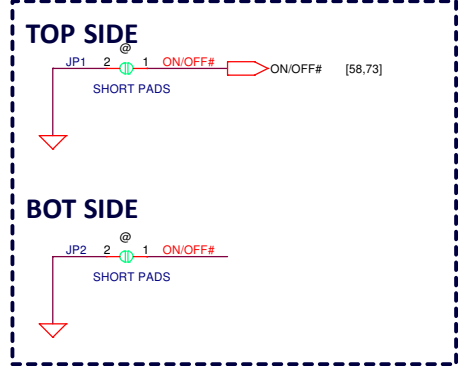
Fiducial Mark



CPU Fan Control Circuit



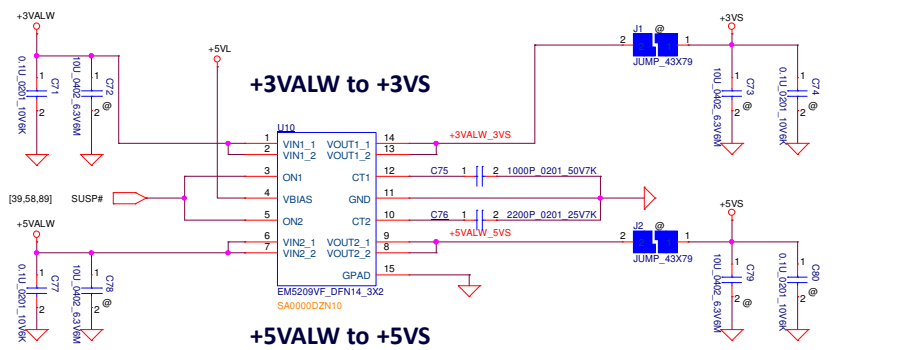
ON/OFF# SHORT PADS



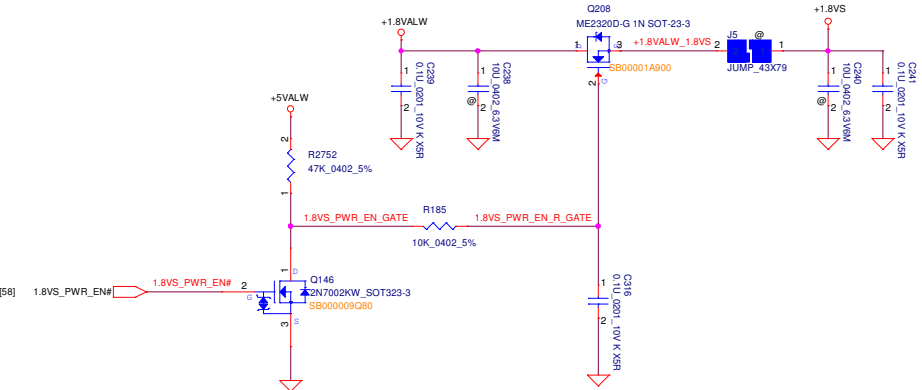
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2020/12/04	Deciphered Date	2020/12/31	Title	PWRBTN/ FAN / Screws
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DC to DC

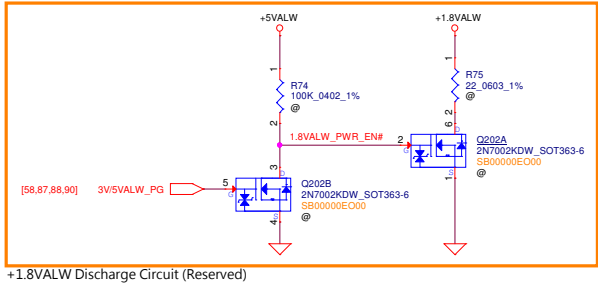
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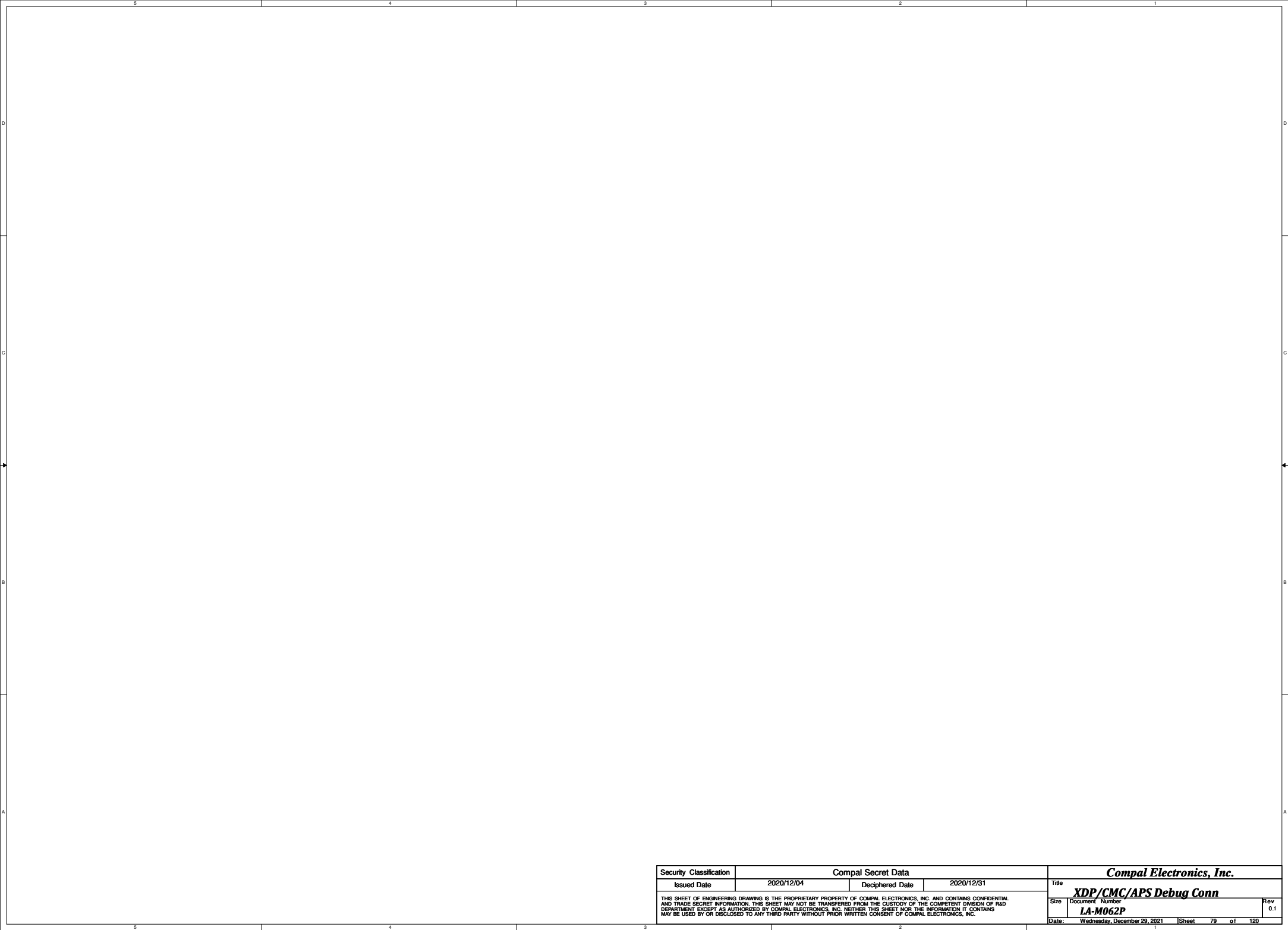


+1.8VALW to +1.8VS



DISCHARGE CIRCUIT





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				Size	Document Number	Rev
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HW SIT PIR List

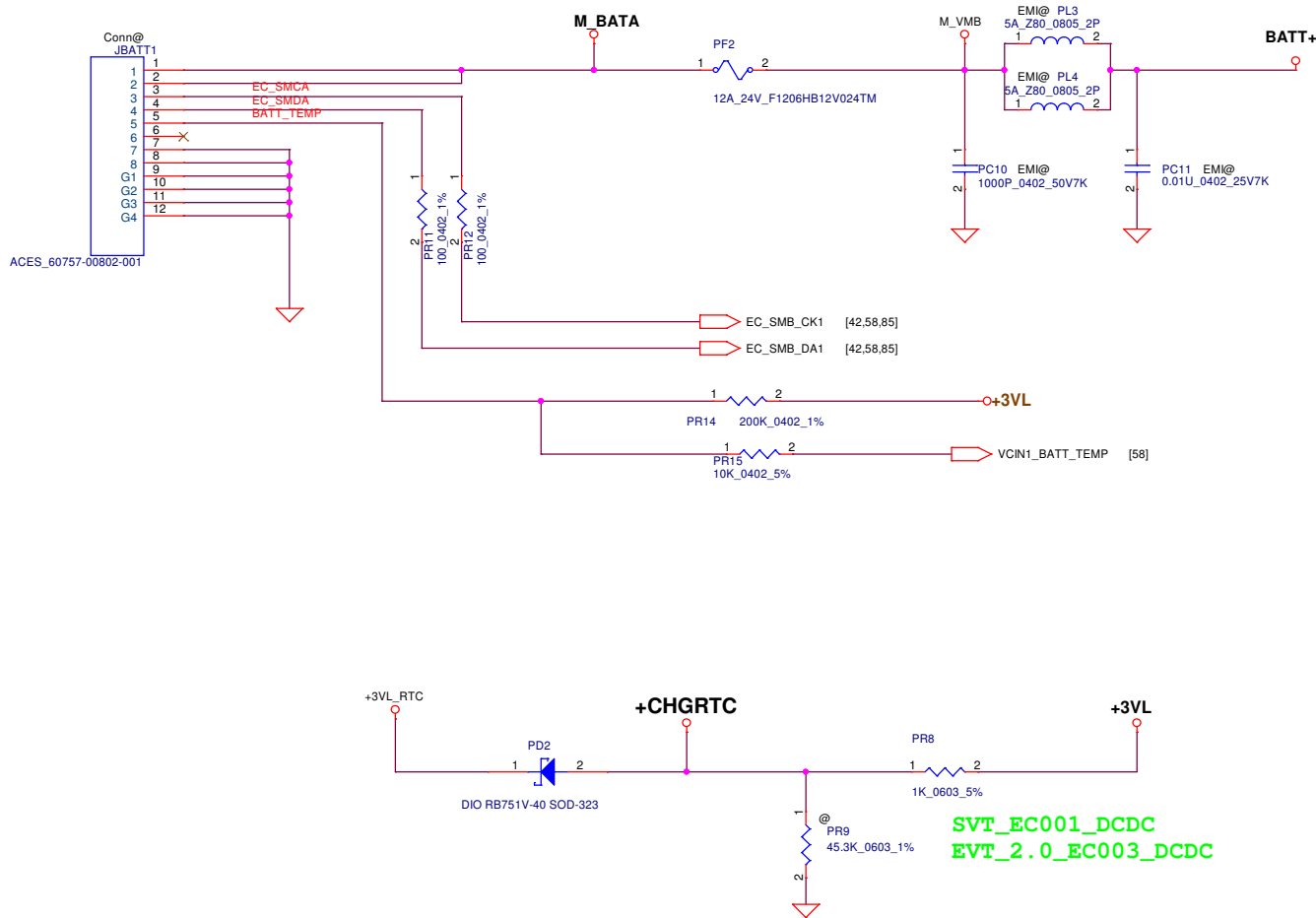
NO	DATE	PAGE	MODIFICATION LIST
1	21/09/30	66	UN2 change to ST IC (PN:SA0000CKQ00), add RN5 and RN6
2	21/10/01	10	delete 32M BIOS ROM(UC4)
3	21/10/15	39	Add CT55&CT56 (EMI request)
4			

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					Size	Document Number			Rev
					LA-M062P	0.1			
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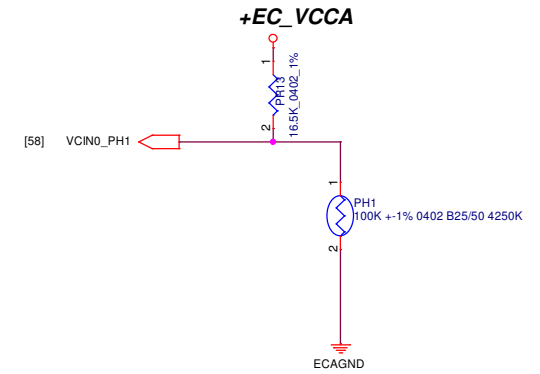


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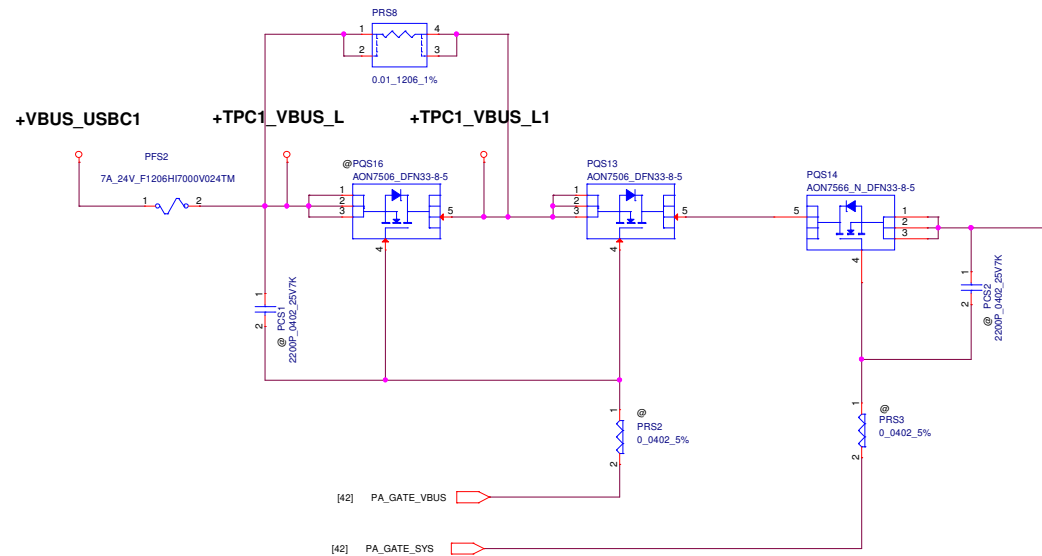
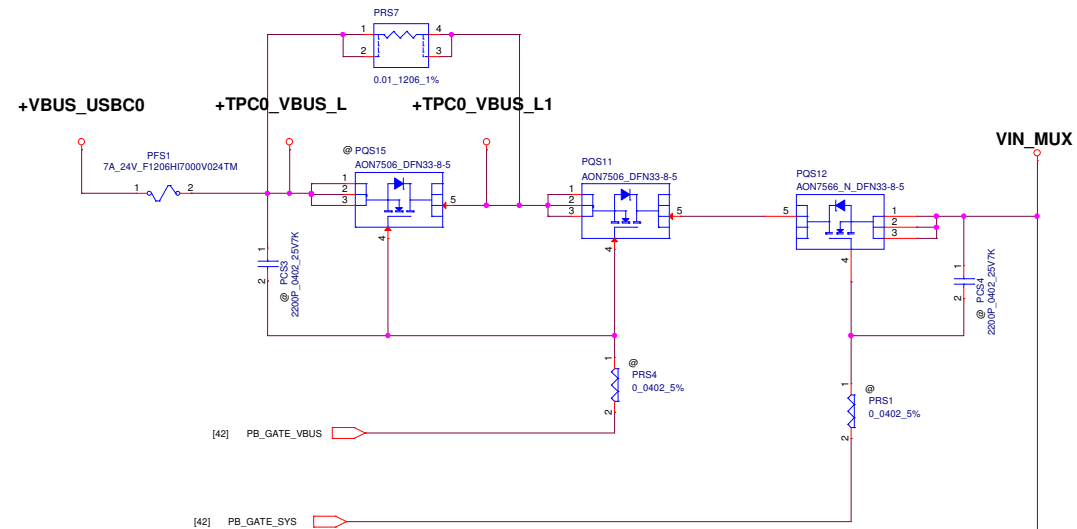
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				Date: Wednesday, December 29, 2021	Rev 0.1
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**PH201 under CPU botten side :**  
**CPU thermal protection at 93 +-3 degree C**  
**Recovery at 56 +-3 degree C**



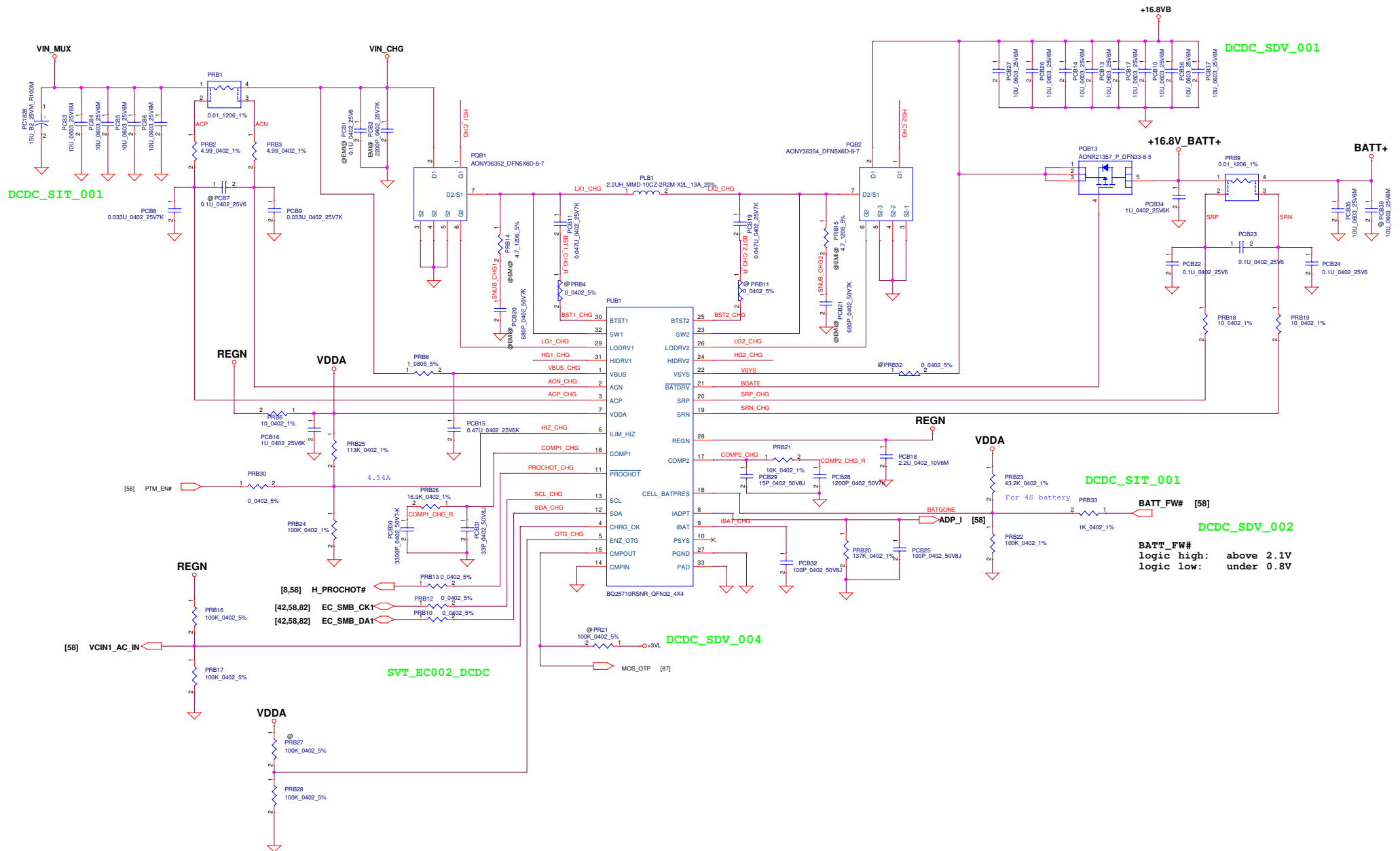
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Issued Date	2021/05/03	Deciphered Date	2021/05/31	Title	PWR- DC Conn/Type-C PD in
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				Custom	LA-M062P
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				Date	Wednesday, December 23, 2021
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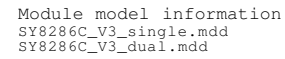
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				Custom	LA-M062P	0.1
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SY8286B\_V3\_single.mdd  
SY8286B\_V3\_dual.mdd



```
Fsw : 600K Hz
EN1 and EN2 dont't be floating.
EN :H>1V ; L<0.4V
```



```
EN1 and EN2 dont't be floating.
EN :H>0.8V ; L<0.4V
```



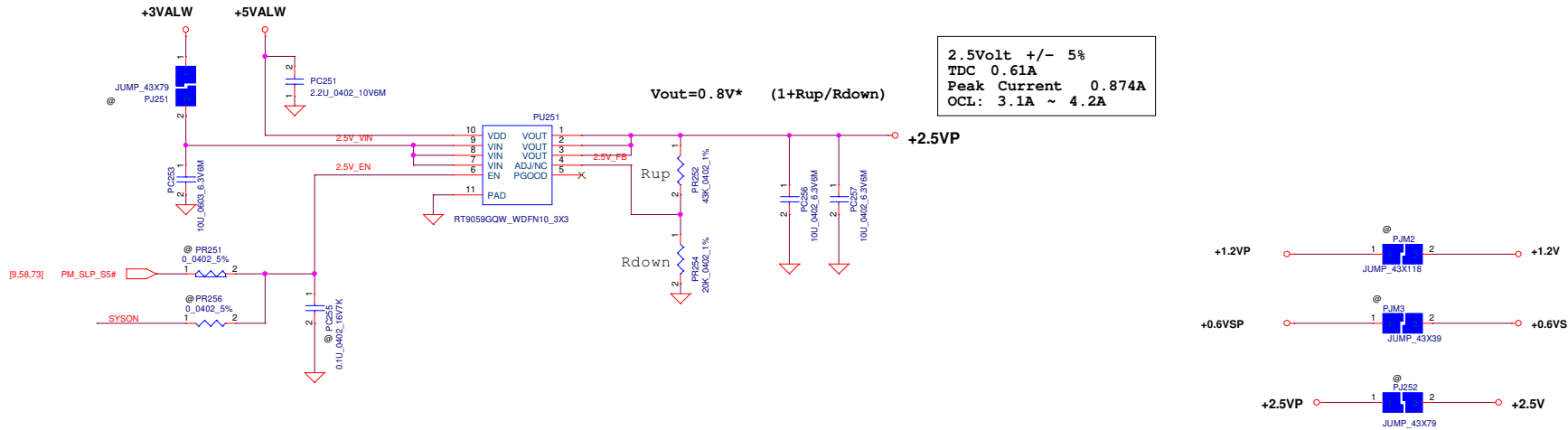
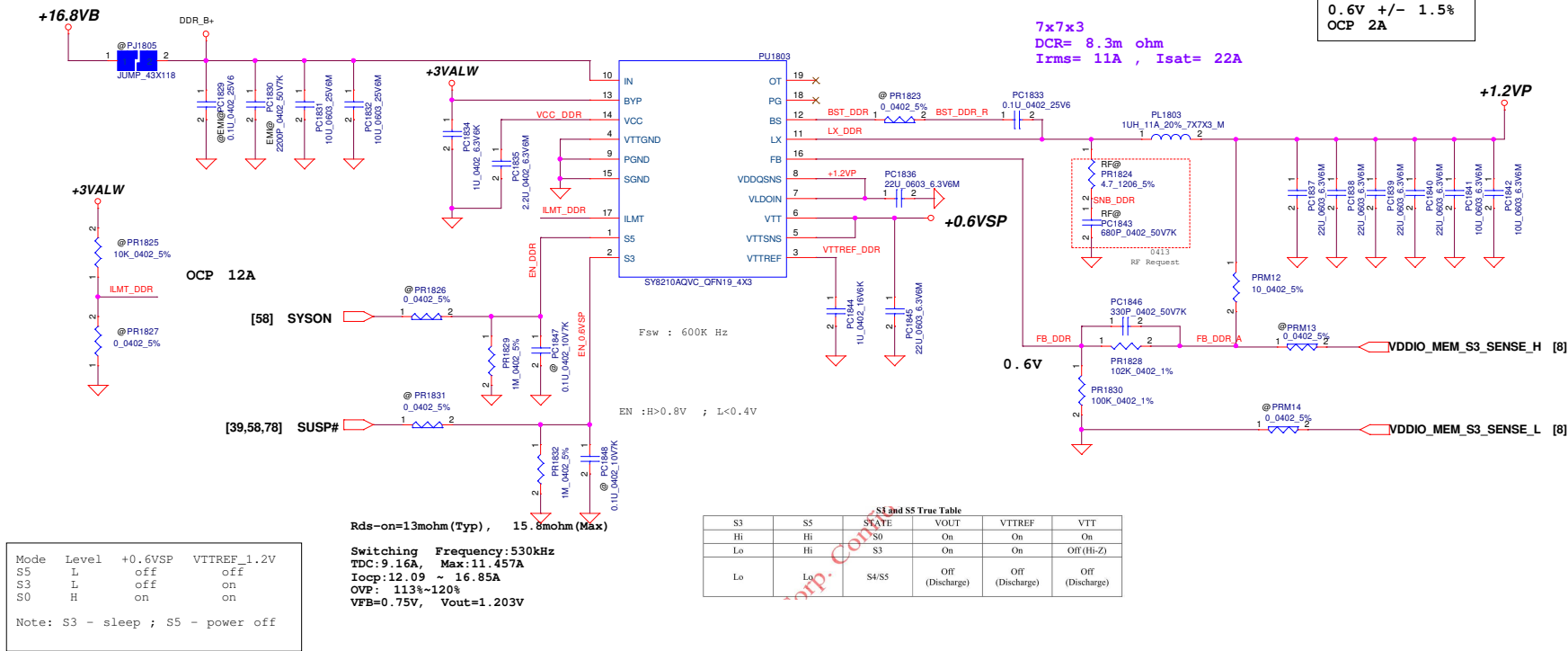
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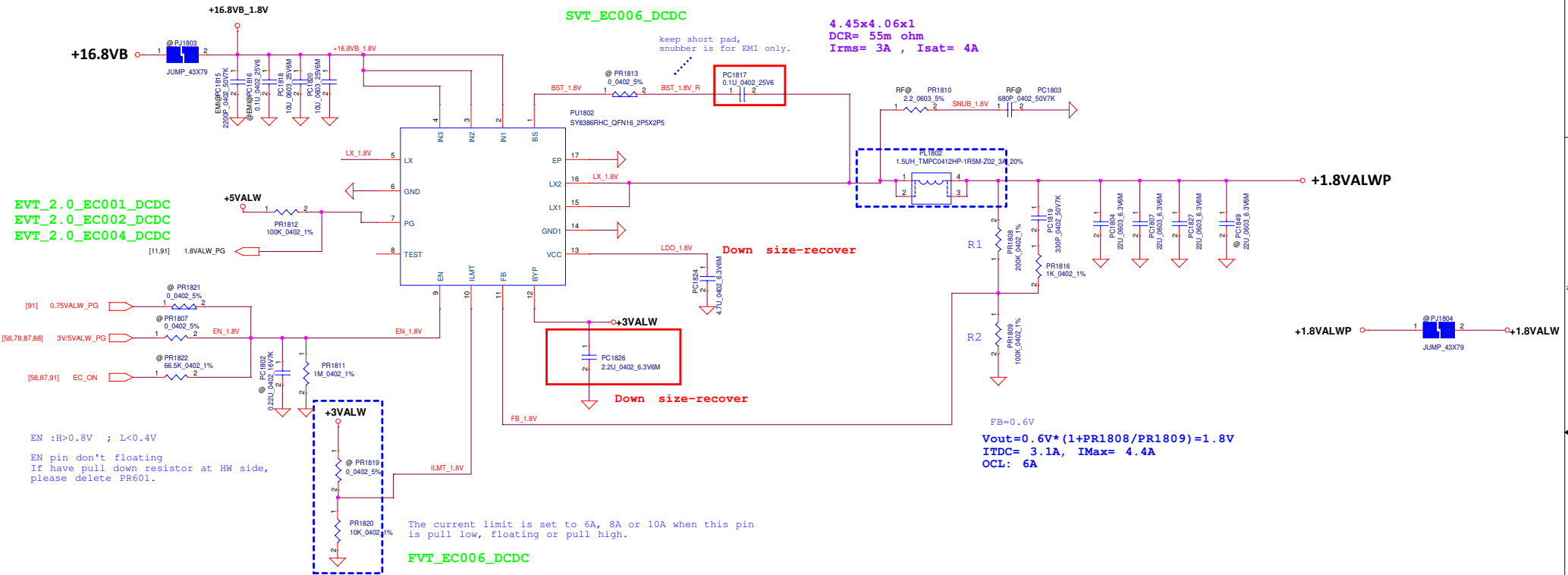
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Date	Wednesday, December 29, 2021		Sheet	87	of 130











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Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2021/05/03	Deciphered Date	2021/05/31	Title	
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				Size	Document Number
				Custom	LA-M062P
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				Size	Document Number
				Custom	LA-M062P
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				Sheet	93 of 120
				Rev	0.1

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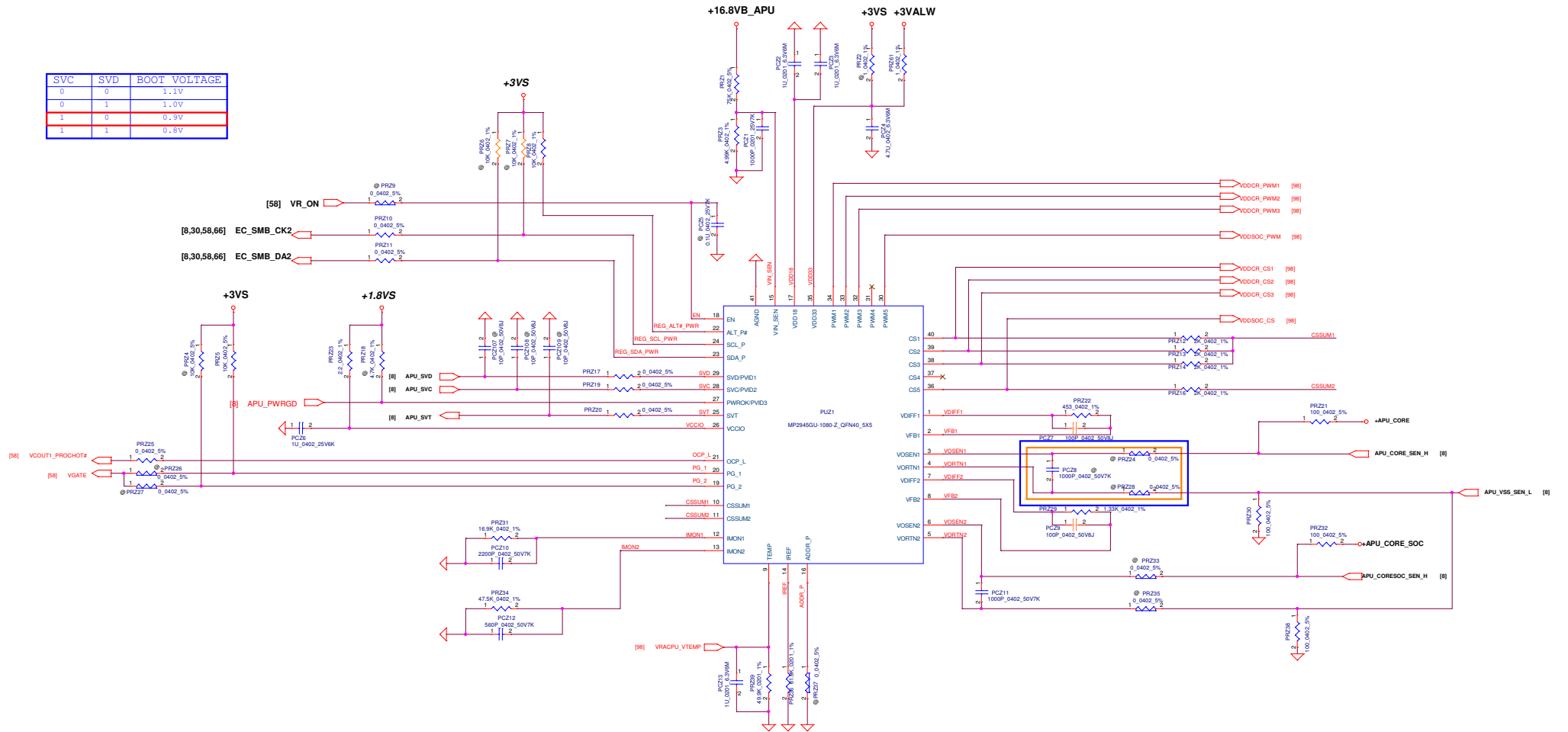
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				Date:	Wednesday, December 29, 2021
				Sheet	95 of 120
				Rev	0.1

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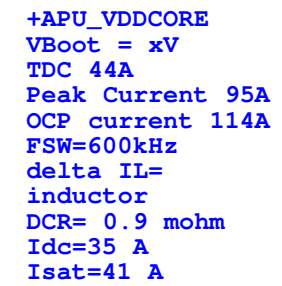
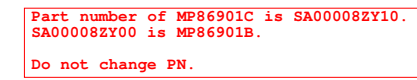
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SVC	SVD	BOOT VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



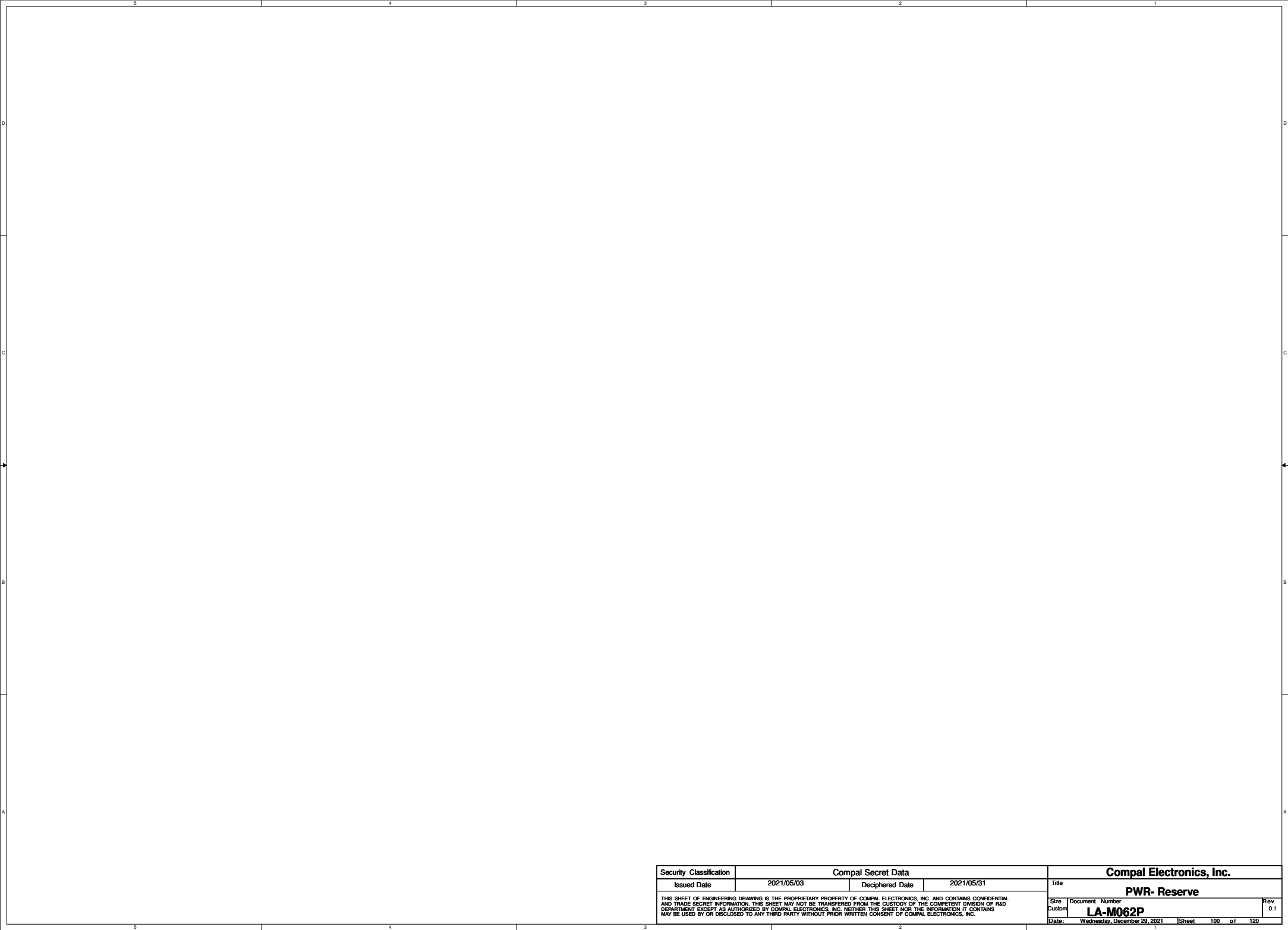
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Size	Document	Number	P088-PWR-APU_CORE(MP2945)	
Date	Wednesday, December 23, 2021	Sheet	97	of 120



Security Classification	<b>Compel Secret Data</b>		<b>Compel Electronics, Inc.</b>	
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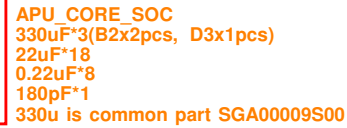
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Issued Date	2021/05/03	Deciphered Date	2021/05/31	Title	PWR- Reserve	
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Date:				Wednesday, December 29, 2021		
				Sheet	99	of 120

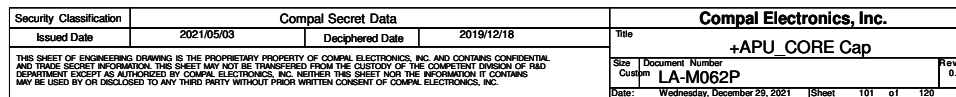


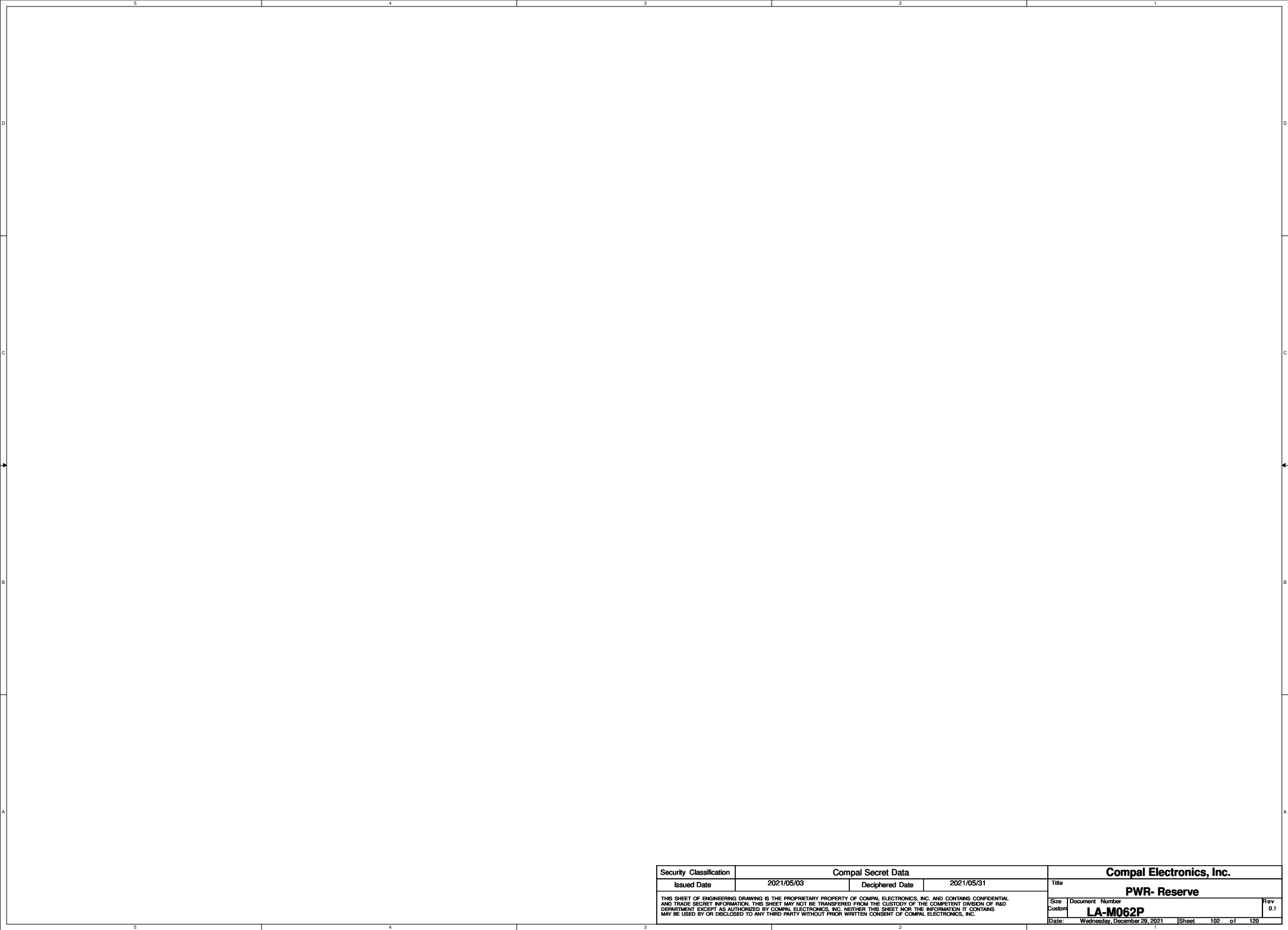
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## +APU\_CORE

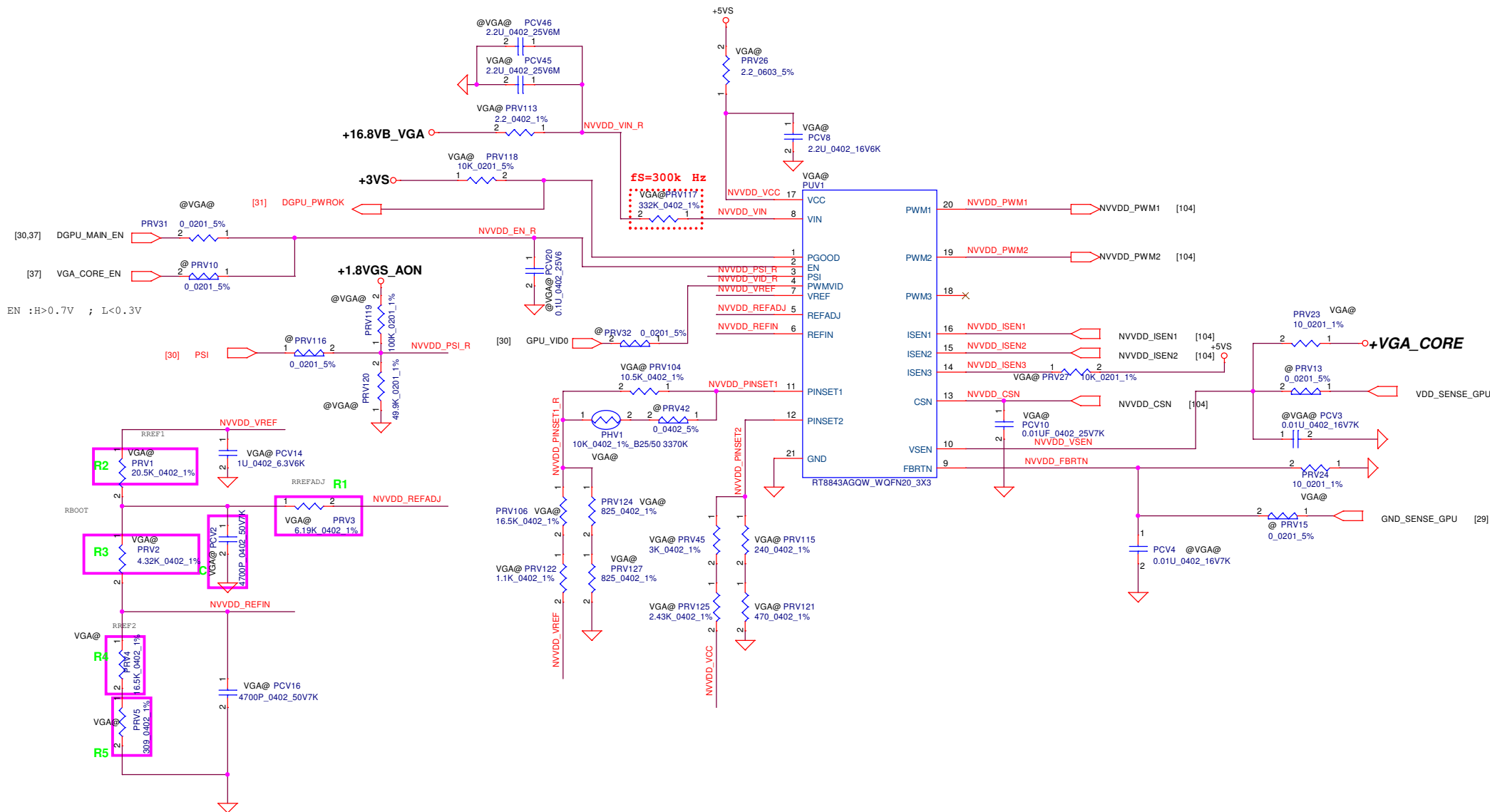


APU CORE  
330uF\*8pcs(B2x6pcs+D3x2pcs)  
220uF \*3(D7x3pcs)  
22uF\*45  
0.22uF\*8  
180pF\*1  
  
B2=1.9h,D3=1.4h, D7=1h  
  
330u is common part SGA00009S00





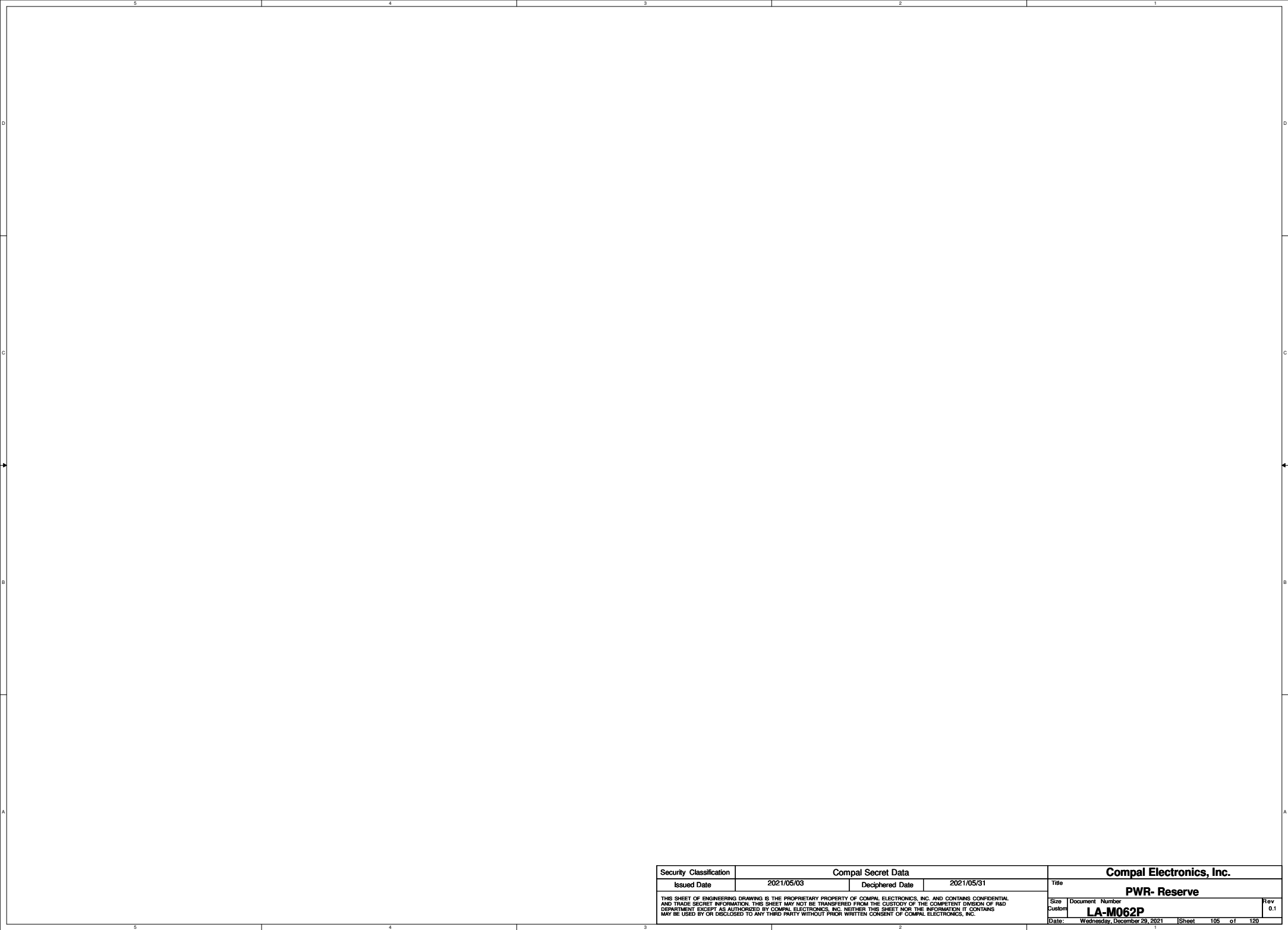
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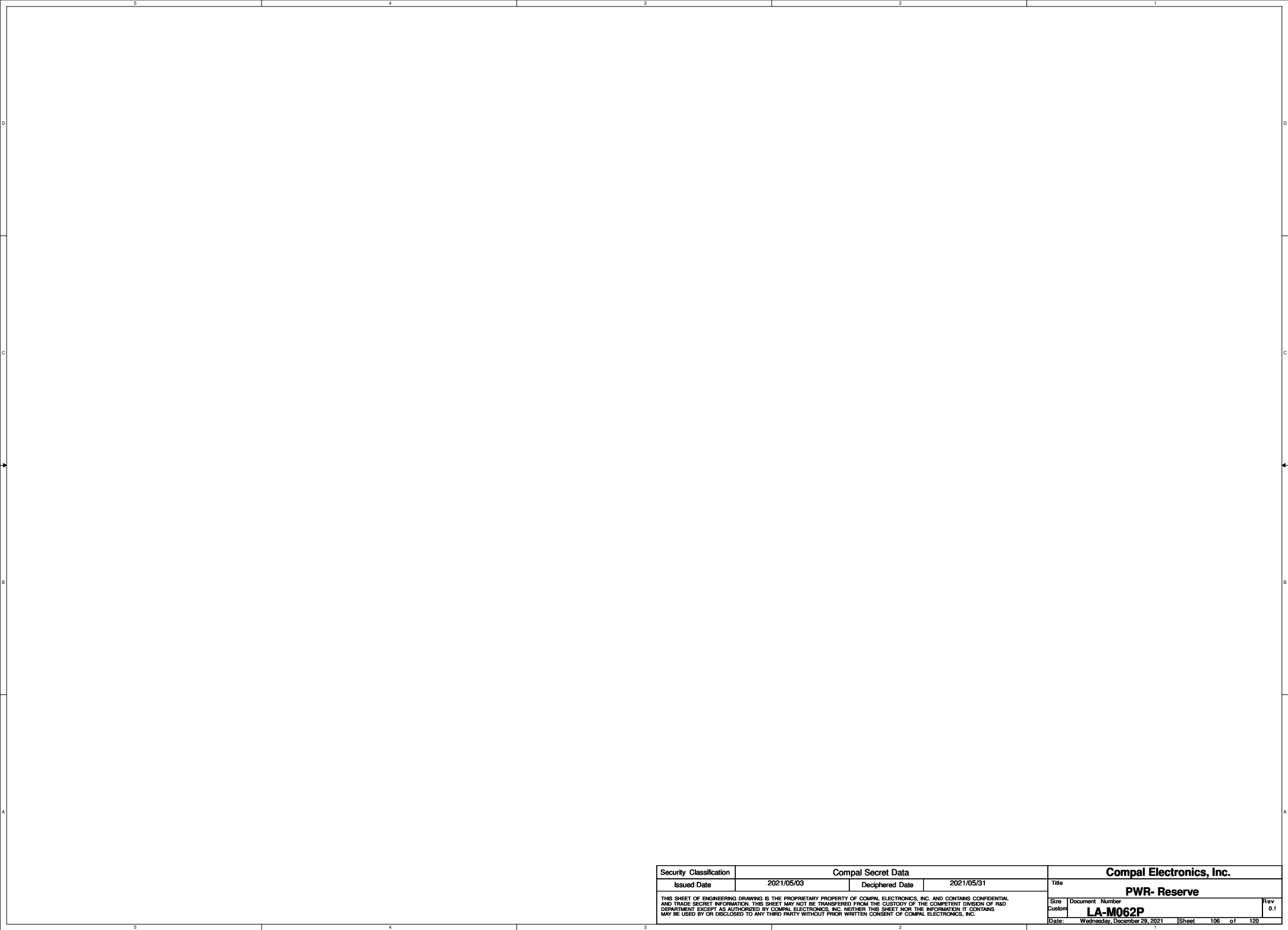
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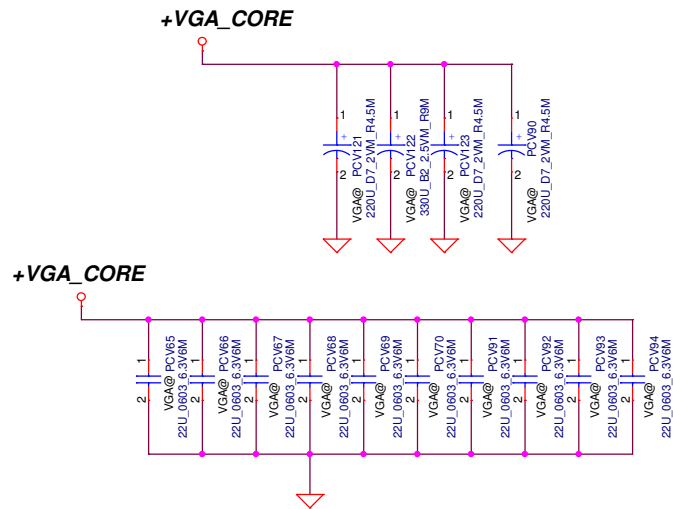




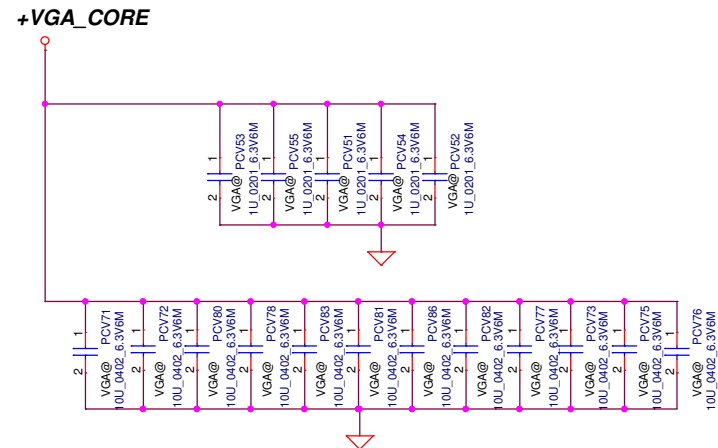
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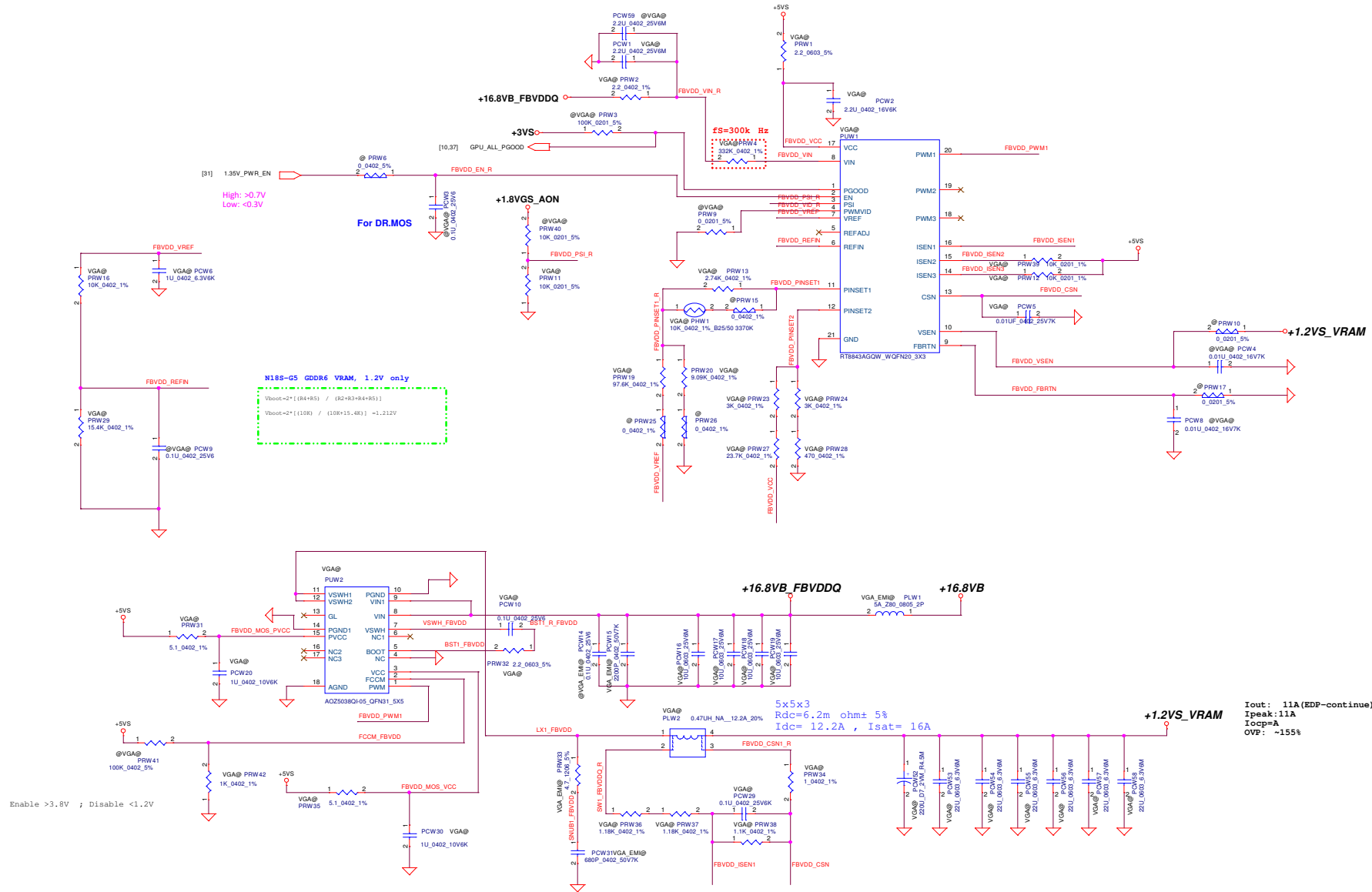
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VGA\_CORE output cap  
 330U\_B2\_2.5V 1pcs  
 220U\_D7\_2.5V 3pcs  
 22U\_0603\_6.3V 10pcs  
 10U\_0603\_6.3V 12pcs  
 1U\_0402\_16V 5pcs



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Size	Custom	Document Number	LA-M062P	Rev	0.1
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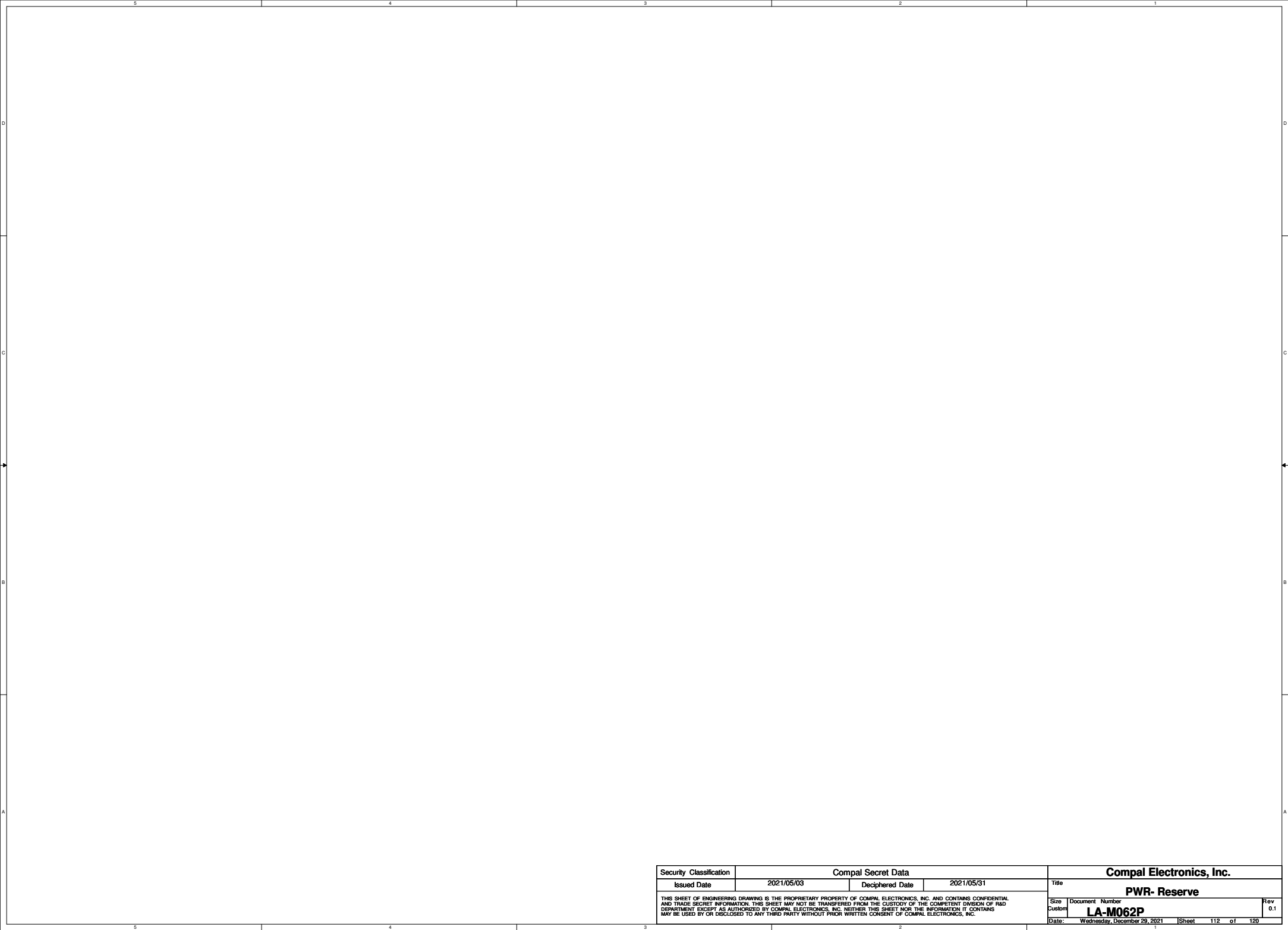


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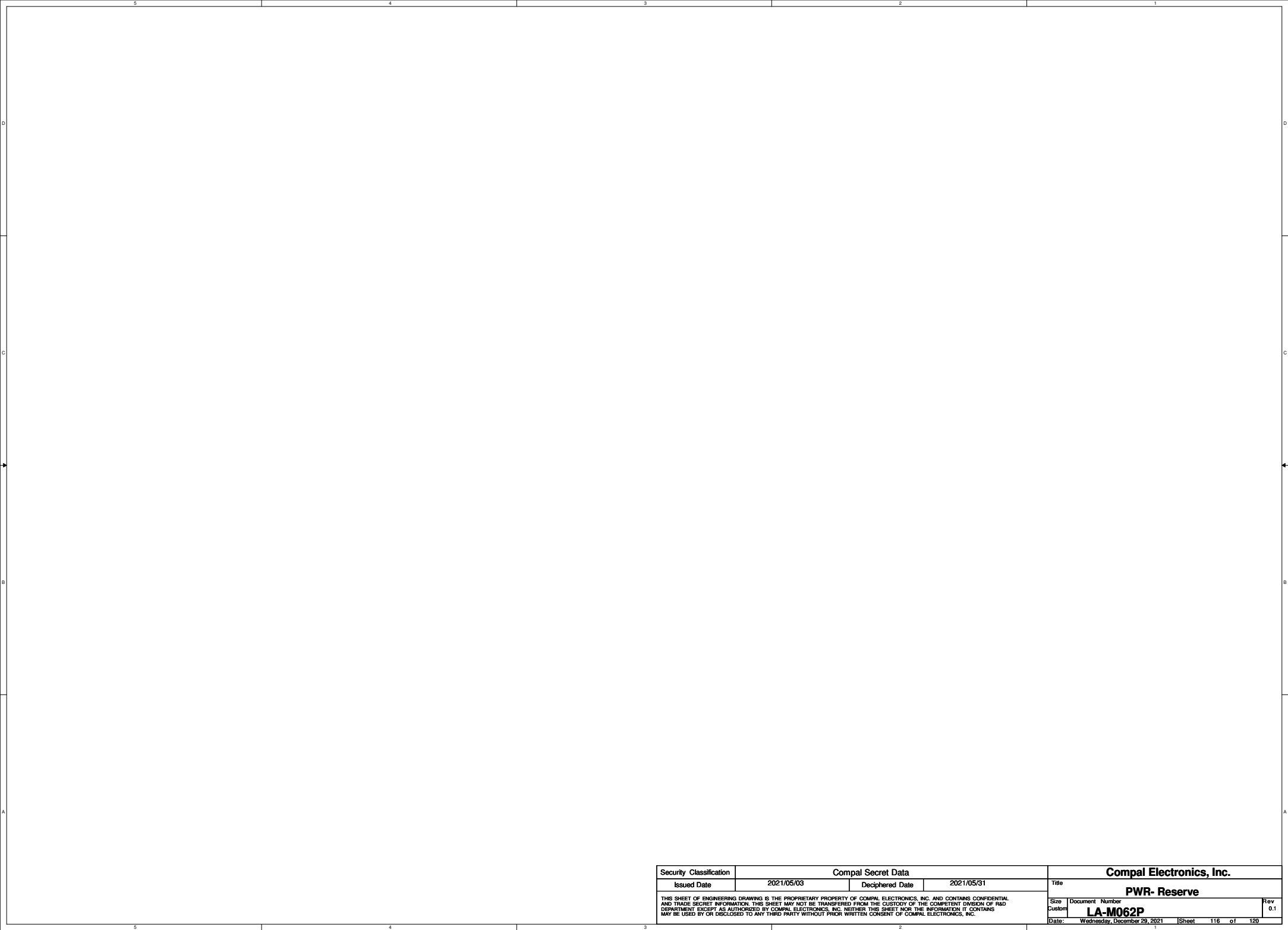
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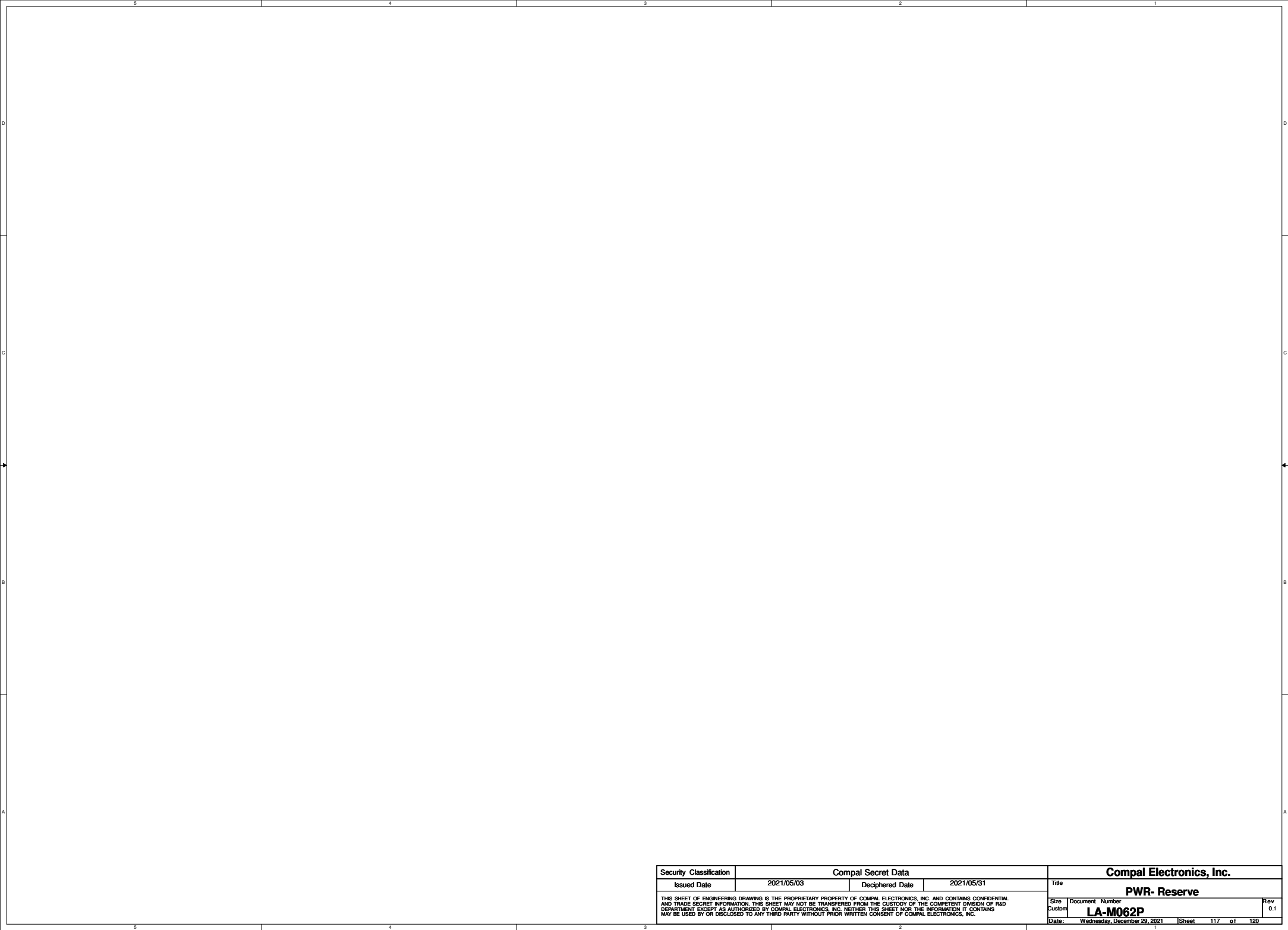
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Item	Reason for change	PG#	Modify List	Date	Phase
EVT 1	For 4 Cell voltage level as Vender suggestion	85	Add two capacitor PCB36 / PCB37 of 10U_0603_25V6M	2020/01/31	A
2	For EC COMMON design as battery FW update feature	85	Add one Oohm (PRB33) and BATT_FW#	2020/01/31	A
3	Tuning PRM5 for 1.2V OCP to 12.6A	89	Tuning PRM5 from 23.7K0402 to 27K_0402(BOM change)	2020/02/04	A
4	For Pull high change	85	PR21 pull high from +3VLP to +3VL	2020/02/04	A
FVT 1	Sequence change	88	PU502.12 change from 5V_3V_EN to 5V_EN	2020/03/19	B
2	Offset 0.75V as test.	91	PRF4, PRF30 from 39.2K to 42.2K	2020/03/19	B
3	Co-lay 3phase ==> CP20200317_0011	97	Change VR controller from RT3662 to RT3663	2020/03/26	B
4	Co-lay 3phase ==> CP20200317_0011	98	Add 3-phase for co-lay	2020/03/26	B
5	Co-lay 3phase ==> CP20200317_0011	101	1. PCZ197, PCZ195, PCZ218 from D2 size to B2 size 2. Reserve 22uF *10 & Polymar cap *1	2020/03/26	B
6	Pull down resistor change from Oohm to 10K	90	PR1820 change from O_0402 ohm to 10K_0402	2020/04/9	B
7	EMI request Snubber	87.88	1. PR502>> 4.7_1206 , PC513 >> 680P_0402 mount 2. PR518>> 4.7_1206 , PC533 >> 680P_0402 mount	2020/04/9	B
8	BOM change for CPU power 3phase sense reserve	97	Unmount PRZ74, PRZ75	2020/04/9	B
SIT 1	Batt_FW pin reserve<FVT SMT MEMO>	85	Mount PRB33 as 1K_0402	2020/06/04	C
2	0.75V remote sense <FVT SMT MEMO>	91	Mount PRF7, PRF25, PRF28, PRF33 Oohm	2020/06/04	C
3	APU APU_CORE_SOC test >> SDLE tuning	97	1. PRZ107 change from 59K_0402 to 68K_0402 2. PCZ248 change from 330P_50V to 390P_50V. 3. PRZ93 change from 9.31K_0402 to 10K_0402. 4. PRZ92 cahnge from 8.25K_0402 to 8.45K_0402.	2020/06/04	C
SVT 1	Shortpad change	82	PR8 chagne from O_0603 to 0603 Shortpad	2020/07/08	Pre-MP
2	Shortpad change	85	PRB10, PRB12, PRB32, PRB4, PRB11 chagne from O_0402 to 0402 Shortpad	2020/07/08	Pre-MP
3	Shortpad change	87	PR511, PR514, PR501, PR301 chagne from O_0402 to 0402 Shortpad	2020/07/08	Pre-MP
4	Shortpad change	88	PR517, PR516 chagne from O_0402 to 0402 Shortpad	2020/07/08	Pre-MP
5	Shortpad change	89	PRM3, PRM4, PR251 chagne from O_0402 to 0402 Shortpad	2020/07/08	Pre-MP
6	Shortpad change	90	PR1813 chagne from O_0402 to 0402 Shortpad	2020/07/08	Pre-MP
7	Shortpad change	91	PRF32, PRF28,PRF33,PRF7,PRF25 chagne from O_0402 to 0402 Shortpad	2020/07/08	Pre-MP
8	Shortpad change	97	PRZ79,PRZ78,PRZ77 chagne from O_0402 to 0402 Shortpad	2020/07/08	Pre-MP
9	For ACS5 consumption optimize	83	1. PRS3, PRS5, PRS8, PRS10chagne from 47K_0402 to 68.1K_0402 2. PRS4, PRS9, PRS1 chagne from 470K_0402 to 681K_0402	2020/07/15	Pre-MP
10	Un-mount reserve part for 3phase	98	Un-mount PRZ68, PCZ219, PCZ253, PCZ223, PCZ222, PRZ71, PCZ225, PRZ69, PCZ224, PRZ70	2020/07/15	Pre-MP
11	Soft-start tuning for Type-C monitor input.	83	PRS2, PRS7 from 49.9K_0402_1% to 121K_0402_1%	2020/07/23	Pre-MP
12	For ACS5 consumption optimize	87	PR303, PR509 from 100K_0402_5% to 300K_0402_1%	2020/07/27	Pre-MP

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